EC–QPJHA–TE

Digital Semiconductor
77 Reed Road
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Dear Customer:

The Digital Semiconductor 21052 PCI-to-PCI Evaluation Kit (21A52-01) contains an early production (Rev. B) 21052 device. The Rev. B device exhibits the interoperability problem with Intel's Trition (#82437) core logic chipset, that is described below.

The Rev. B device can be identified by the marking "21-43698-01".

A redesign of the 21052 has been completed and production of Rev. C has begun. As a result of this change the deadlock will not occur with Rev. C of the 21052.

Samples of the 21052 Rev. C will be available in early September with volume availability occurring late September. Rev. B of the 21052 is available today and can be used in designs not impacted by this issue or can be used for design and development purposes until the Rev. C is available.

This deadlock occurs between the 21052 Rev. B and the Triton chipset when the following sequence of events happens:

1. Write data is posted in the 21052's upstream buffers by a device on the secondary bus. The 21052 asserts its primary bus request.
2. Before this upstream data can be delivered to the primary bus target, typically to system memory, Triton posts write data in the 21052's downstream data buffers.
3. At this point, the 21052 must be allowed to initiate the upstream transaction before the delivery of downstream data can be attempted. This is because the 21052 only drives one PCI interface at a time in order to reduce switching noise. The 21050 uses a fixed method of delivering posted write data. When data is posted in both upstream and downstream data buffers, it must attempt to deliver the data which was posted first. If the write attempt results in a target retry, then the 21052 will attempt to deliver data in the opposite direction.
4. If the Triton chip has additional data in its posted write buffers, the Triton primary bus arbiter will retain the grant and not allow any other device to use the primary bus. In this case, Triton has multiple posted write transactions in its buffers and does not give up the grant even between delivery of these transactions. Therefore, even though Triton has already posted one transaction to the 21052, it does not allow the 21052 to use the primary bus.

> Because the 21052 cannot obtain access to the primary bus, it cannot initiate the upstream posted write transaction. Because it cannot initiate this transaction, it does not deliver the downstream posted write data. When Triton initiates a transaction to post additional downstream writes, the 21052 returns a target retry in response as it already has data in its downstream buffers. Without allowing other devices to use the primary bus, Triton will make repeated attempts to post this additional write data resulting in a deadlock.

Please contact your Digital Semiconductor Sales Representative for further information and support.

Sincerely,

George Falvella, Product Manager