DECchip 21140A PCI Fast Ethernet LAN Controller

Data Sheet

Order Number: EC–QN7PA–TE

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1 DECchip 21140A Overview

The DECchip 21140A PCI Fast Ethernet LAN Controller (21140A) supports the peripheral component interconnect (PCI) bus. It provides a direct interface connection to the PCI and adapts easily to most other standard buses. The 21140A software interface and data structures are optimized to minimize the host CPU load and to allow for maximum flexibility in the buffer descriptor management. The 21140A contains large onchip FIFOs, so no additional onboard memory is required. The 21140A provides an upgradable boot ROM interface.

The DECchip 21140A has several additional features that are not available on the DECchip 21140, yet it remains pin and software compatible with the DECchip 21140.

1.1 General Description

The 21140A interfaces with the PCI bus by using onchip control and status registers (CSRs), and a shared CPU memory area that is set up mainly during initialization. This minimizes the processor involvement in the 21140A operation during normal reception and transmission. Traffic on the PCI bus is also minimized by filtering out received runt frames and by automatically retransmitting collided frames without needing to repeat a fetch from shared memory. The 21140A is compliant with the *PCI Local Bus Specification, Revision 2.1*.

On the network side, the 21140A provides two ports: a serial standard 7-wire (SRL) 10Mb/s port and a media-independent interface/symbol (MII/SYM) 10/100Mb/s port. The 10Mb/s port provides a direct interface to the external 10Mb/s front-end decoder (ENDEC). The 10/100Mb/s port supports two operational modes:

- A direct interface to the external 10/100Mb/s ENDEC. The 21140A includes the onchip physical coding sublayer (PCS) and the scrambler for efficient 100BASE-T (CAT5 cable) implementation.
- A full implementation of the MII standard.

The 21140A is also capable of functioning in a full-duplex environment for both the 10Mb/s and 10/100Mb/s ports.

1.2 Features

The 21140A has the following features:

- Offers a single-chip Fast Ethernet controller for PCI local bus:
  - Provides a glue-less connection to the PCI bus
  - Supports two network ports: 10Mb/s and 10/100Mb/s
- Provides a standard 10/100Mb/s MII supporting CAT3 unshielded twisted-pair (UTP), CAT5 UTP, shielded twisted-pair (STP) and fiber cables
- Contains onchip scrambler and PCS for CAT5 to significantly reduce cost of 100BASE-T solutions
- Supports full-duplex operation on both 10Mb/s and 10/100Mb/s ports
- Provides external and internal loopback capability on both ports
- Contains a variety of flexible address filtering modes (including perfect, hash tables, inverse perfect, and promiscuous):
  - 16 perfect addresses (normal or inverse filtering)
  - 512 hash-filtered addresses
  - 512 hash-filtered multicast addresses and one perfect address
  - Pass all multicast
  - Promiscuous
  - Pass all incoming packets with a status report[1]
- Offers a unique, patented solution to Ethernet capture-effect problem
- Contains large independent receive and transmit FIFOs; no additional onboard memory required
- Includes a powerful onchip direct memory access (DMA) with programmable burst size providing for low CPU utilization
- Implements unique, patent-pending intelligent arbitration between DMA channels preventing underflow or overflow
- Supports PCI clock frequency from dc to 33 MHz; network operational with PCI clock from 20 MHz to 33 MHz
- Supports an unlimited PCI burst
- Supports PCI read multiple command[1]

[1] Indicates DECchip 21140A features that are not available on the DECchip 21140.

- Supports early interrupts on transmit[1]
- Implements low-power management with two power-saving modes (sleep or snooze)[1]
- Supports both PCI 5.0-V and 3.3-V signaling environments[1]
- Supports either big or little endian byte ordering for buffers and descriptors
- Contains 8-bit, general-purpose, programmable register and corresponding I/O pins
- Provides LED support for various network activity indications
- Provides MicroWire interface for serial ROM (1K and 4K EEPROM)
- Provides an upgradable boot ROM (flash or EEPROM) interface of up to 256KB[1]
- Supports automatic loading of subvendor ID configuration register[1]
- Implements JTAG-compatible test-access port with boundary-scan pins
- Supports IEEE 802.3, ANSI 8802-3, and Ethernet standards
- Implements low-power, 3.3-V complementary metal-oxide semiconductor (CMOS) process technology

1.3 Microarchitecture

The following list describes the 21140A hardware components, and Figure 1 shows a block diagram of the 21140A:

- PCI interface—Includes all interface functions to the PCI bus; handles all interconnect control signals; and executes PCI DMA and I/O transactions.
- DMA—Contains dual receive and transmit controller; supports bursts of up to 32 longwords; handles data transfers between CPU memory and onchip memory.
- FIFOs—Contains two FIFOs for receive and transmit; supports automatic packet deletion on receive (runt packets or after a collision) and packet retransmission after a collision on transmit.
- TxM—Handles all CSMA/CD[2] MAC[3] transmit operations, and transfers data from transmit FIFO to the ENDEC for transmission.

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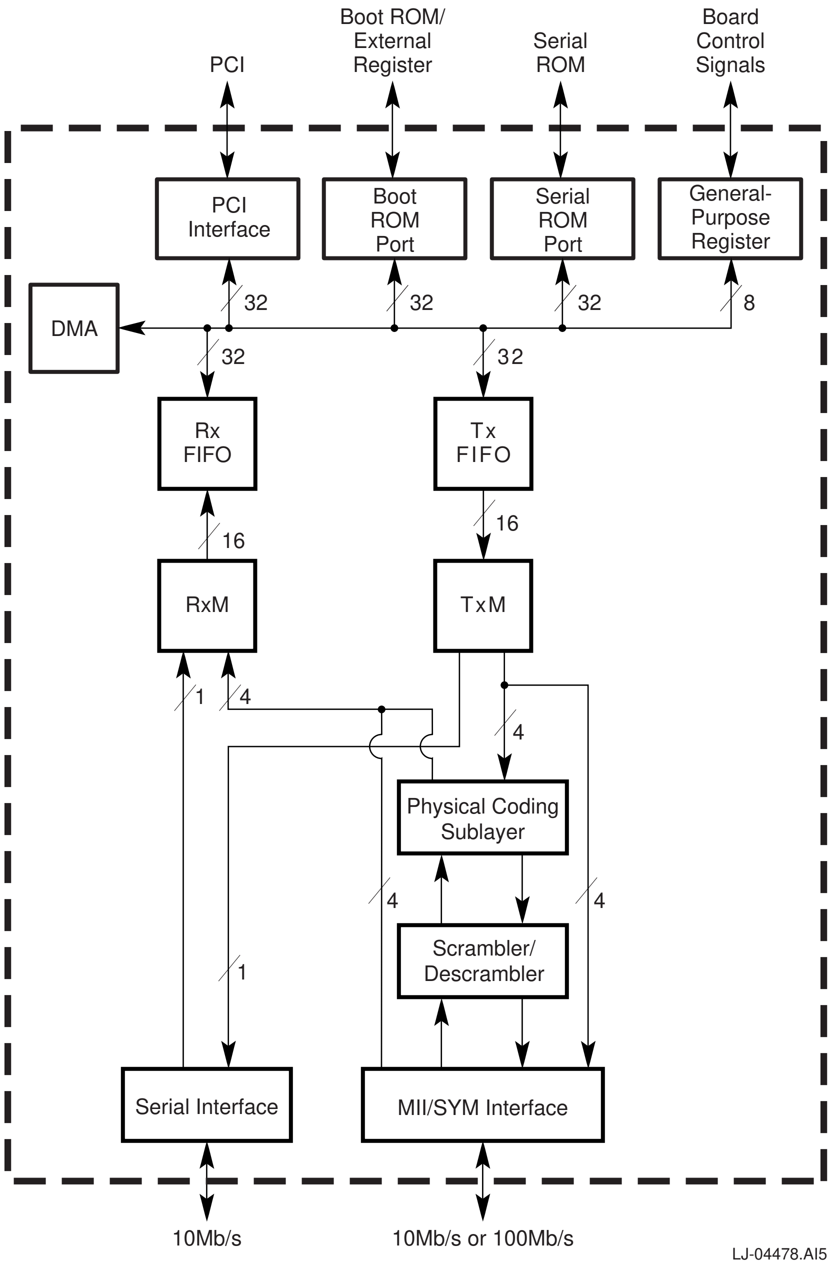
1 Indicates DECchip 21140A features that are not available on the DECchip 21140.
2 Carrier-sense multiple access with collision detection
3 Media access control

- RxM—Handles all CSMA/CD receive operations, and transfers the data from the ENDEC to the receive FIFO.
- Physical coding sublayer—Implements the encoding and decoding sublayer of the 100BASE-TX (CAT5) specification, including the squelch.
- Scrambler/descrambler—Implements the twisted-pair physical layer medium dependent (TP-PMD) scrambler/descrambler scheme.
- General-purpose register—Enables software to use for input or output functions.
- Serial interface—Provides a 7-wire conventional interface to the Ethernet ENDEC components.
- MII/SYM interface— Provides a full MII signal interface and a direct interface to the 10/100Mb/s ENDEC for CAT5.
- Serial ROM—Provides a direct interface to the MicroWire Ethernet address ROM and system parameters.
- Boot ROM—Includes the required interface to the boot ROM for read and write operations; supports accesses to bytes or longword (32-bit). Also provides the ability to connect an external 8-bit register to the boot ROM port.

Figure 1 DECchip 21140A Block Diagram



2 Pinout

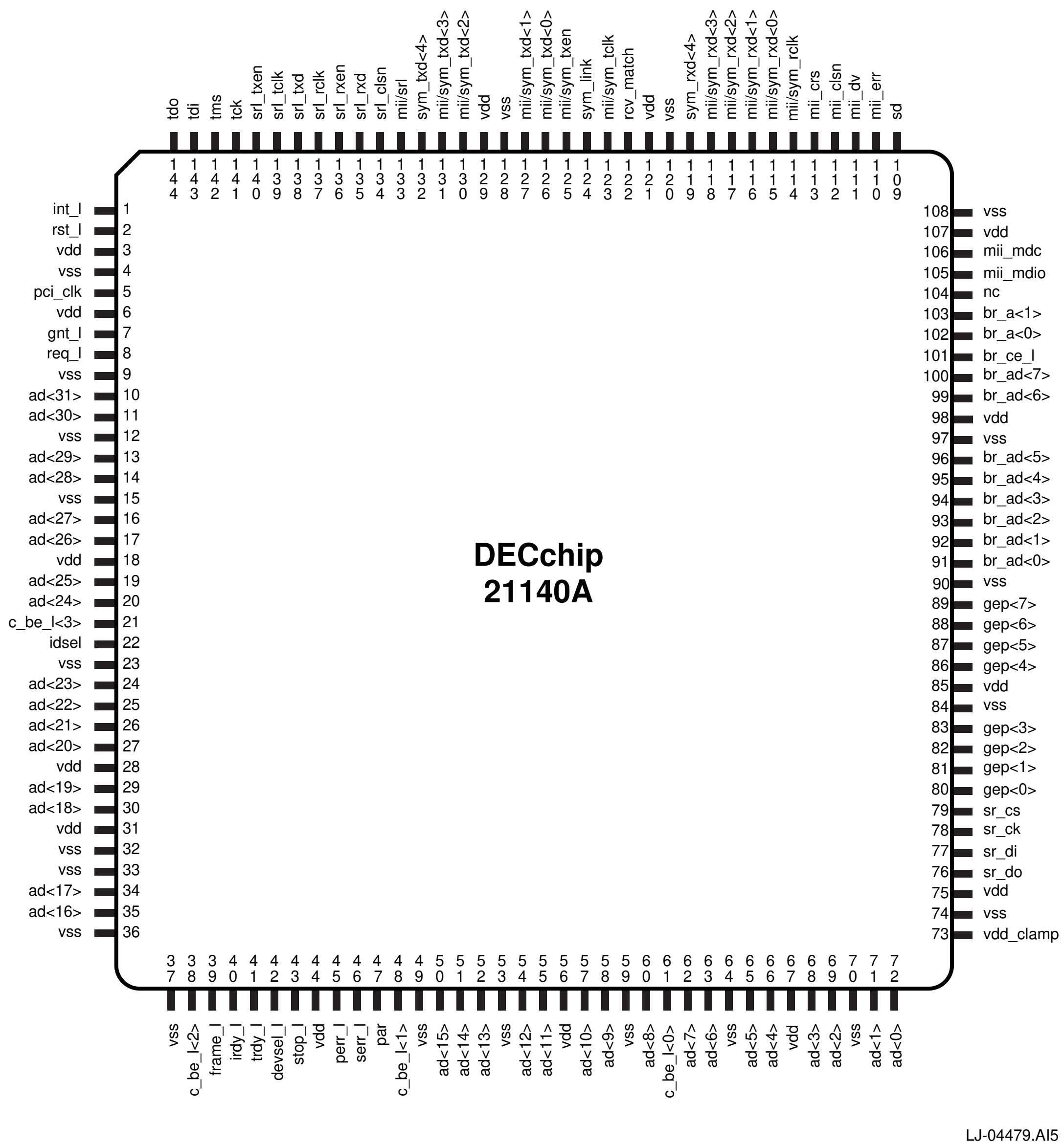
The 21140A is packaged in a 144-pin plastic quad flat pack (PQFP). The tables in this section provide a description of the pins and their respective signal definitions.

Table 1 lists the tables in this section. Figure 2 shows the 21140A pinout.

Table 1 Index to Pinout Tables

For this information . . .	Refer to . . .
Logic signals	Table 2
Power pins	Table 3
Functional signals description	Table 4
Input pins	Table 5
Output pins	Table 6
Input/output pins	Table 7
Open drain pins	Table 8
Signal functions	Table 9

Figure 2 DECchip 21140A Pinout Diagram (Top View)



2.1 Signal Reference Tables

Table 2 provides an alphabetical list of the 21140A logic names and their pin numbers. Table 3 provides a list of the 21140A power pin numbers.

Table 2 Logic Signals

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
ad<0>	72	**ad<24>**	20	**frame_l**	39
ad<1>	71	**ad<25>**	19	**gep<0>**	80
ad<2>	69	**ad<26>**	17	**gep<1>**	81
ad<3>	68	**ad<27>**	16	**gep<2>**	82
ad<4>	66	**ad<28>**	14	**gep<3>**	83
ad<5>	65	**ad<29>**	13	**gep<4>**	86
ad<6>	63	**ad<30>**	11	**gep<5>**	87
ad<7>	62	**ad<31>**	10	**gep<6>**	88
ad<8>	60	**br_a<0>**	102	**gep<7>**	89
ad<9>	58	**br_a<1>**	103	**gnt_l**	7
ad<10>	57	**br_ad<0>**	91	**idsel**	22
ad<11>	55	**br_ad<1>**	92	**int_l**	1
ad<12>	54	**br_ad<2>**	93	**irdy_l**	40
ad<13>	52	**br_ad<3>**	94	**mii_clsn**	112
ad<14>	51	**br_ad<4>**	95	**mii_crs**	113
ad<15>	50	**br_ad<5>**	96	**mii_dv**	111
ad<16>	35	**br_ad<6>**	99	**mii_err**	110
ad<17>	34	**br_ad<7>**	100	**mii_mdc**	106
ad<18>	30	**br_ce_l**	101	**mii_mdio**	105
ad<19>	29	**c_be_l<0 >**	61	**mii/srl**	133
ad<20>	27	**c_be_l<1 >**	48	**mii/sym_rclk**	114
ad<21>	26	**c_be_l<2 >**	38	**mii/sym_rxd<0>**	115
ad<22>	25	**c_be_l<3 >**	21	**mii/sym_rxd<1>**	116
ad<23>	24	**devsel_l**	42	**mii/sym_rxd<2>**	117

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Table 2 (Cont.) Logic Signals

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
mii/sym_rxd<3>	118	**req_l**	8	**srl_tclk**	139
mii/sym_tclk	123	**rst_l**	2	**srl_txd**	138
mii/sym_txd<0>	126	**sd**	109	**srl_txen**	140
mii/sym_txd<1>	127	**serr_l**	46	**stop_l**	43
mii/sym_txd<2>	130	**sr_ck**	78	**sym_link**	124
mii/sym_txd<3>	131	**sr_cs**	79	**sym_rxd<4>**	119
mii/sym_txen	125	**sr_di**	77	**sym_txd<4>**	132
nc	104	**sr_do**	76	**tck**	141
par	47	**srl_clsn**	134	**tdi**	143
pci_clk	5	**srl_rclk**	137	**tdo**	144
perr_l	45	**srl_rxd**	135	**tms**	142
rcv_match	122	**srl_rxen**	136	**trdy_l**	41

Table 3 Power Pins

Signal	Pin Numbers	Signal	Pin Numbers
vdd (3.3 V)	3, 6, 18, 28, 31, 44, 56, 67, 75, 85, 98, 107, 121, 129	**vss** (GND)	4, 9, 12, 15, 23, 32, 33, 36, 37, 49, 53, 59, 64, 70, 74, 84, 90, 97, 108, 120, 128
vdd_clamp (5.0 V)	73		

Table 4 provides a functional description of each of the 21140A signals. These signals are listed alphabetically. The functional grouping of each pin is listed in Section 2.3.

The following terms describe the 21140A pinout:

- **Address phase**

  Address and appropriate bus commands are driven during this cycle.

- **Data phase**

  Data and the appropriate byte enable codes are driven during this cycle.

- **_l**

  All pin names with the _l suffix are asserted low.

The following abbreviations are used in Table 4:

I = Input
O = Output
I/O = Input/output
O/D = Open drain
P = Power

Table 4 Functional Description of DECchip 21140A Signals

Signal	Type	Pin Number	Description
ad<31:0>	I/O	See Table 2.	32-bit PCI address and data lines. Address and data bits are multiplexed on the same pins. During the first clock cycle of a transaction, the address bits contain a physical address (32 bits). During subsequent clock cycles, these same lines contain 32 bits of data. A 21140A bus transaction consists of an address phase followed by one or more data phases. The 21140A supports both read and write bursts (in master operation only). Little and big endian byte ordering can be used.
br_a<0>	O	102	Boot ROM address line bit 0. In a 256KB configuration, this pin also carries in two consecutive address cycles, boot ROM address bits 16 and 17.

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Table 4 (Cont.) Functional Description of DECchip 21140A Signals

Signal	Type	Pin Number	Description
br_a<1>	O	103	Boot ROM address line bit 1. This pin also latches the boot ROM address and control lines by the two external latches.
br_ad<7:0>	I/O	See Table 2.	Boot ROM address and data multiplexed lines bits 7 through 0. In the first of two consecutive address cycles, these lines contain the boot ROM address bits 7 through 2, **oe_l** and **we_l**; followed by boot ROM address bits 15 through 8 in the second cycle. During the data cycle, bits 7 through 0 contain data. During operation with the external register, these lines are used to carry data bits 7 through 0 to and from the external register.
br_ce_l	O	101	Boot ROM or external register chip enable.
c_be_l<3:0>	I/O	See Table 2.	Bits 0 through 3 of the bus command and byte enable lines. Bus command and byte enable are multiplexed on the same PCI pins. During the address phase of the transaction, these 4 bits provide the bus command. During the data phase, these 4 bits provide the byte enable. The byte enable determines which byte lines carry valid data. For example, bit 0 applies to byte 0, and bit 3 applies to byte 3.
devsel_l	I/O	42	Device select is asserted by the target of the current bus access. When the 21140A is the initiator of the current bus access, it expects the target to assert **devsel_l** within five bus cycles, confirming the access. If the target does not assert **devsel_l** within the required bus cycles, the 21140A aborts the cycle. To meet the timing requirements, the 21140A asserts this signal in a medium speed (within two bus cycles).

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Table 4 (Cont.) Functional Description of DECchip 21140A Signals

Signal	Type	Pin Number	Description
frame_l	I/O	39	The **frame_l** signal is driven by the 21140A (bus master) to indicate the beginning and duration of an access. The **frame_l** signal asserts to indicate the beginning of a bus transaction. While **frame_l** is asserted, data transfers continue. The **frame_l** signal deasserts to indicate that the next data phase is the final data phase transaction.
gep<7:0>	I/O	See Table 2.	General-purpose pins can be used by software as either status pins or control pins. These pins can be configured by software to perform either input or output functions.
gnt_l	I	7	Bus grant asserts to indicate to the 21140A that access to the bus is granted.
idsel	I	22	Initialization device select asserts to indicate that the host is issuing a configuration cycle to the 21140A.
int_l	O/D	1	Interrupt request asserts when one of the appropriate bits of CSR5 sets and causes an interrupt, provided that the corresponding mask bit in CSR7 is not asserted. Interrupt request deasserts by writing a 1 into the appropriate CSR5 bit. If more than one interrupt bit is asserted in CSR5 and the host does not clear all input bits, the 21140A deasserts **int_l** for one cycle to support edge-triggered systems. This pin must be pulled up by an external resistor.

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Table 4 (Cont.) Functional Description of DECchip 21140A Signals

Signal	Type	Pin Number	Description
irdy_l	I/O	40	Initiator ready indicates the bus master's ability to complete the current data phase of the transaction. A data phase is completed on any rising edge of the clock when both **irdy_l** and target ready **trdy_l** are asserted. Wait cycles are inserted until both **irdy_l** and **trdy_l** are asserted together. When the 21140A is the bus master, **irdy_l** is asserted during write operations to indicate that valid data is present on the 32-bit **ad** lines. During read operations, the 21140A asserts **irdy_l** to indicate that it is ready to accept data.
mii_clsn	I	112	Collision detected is asserted when detected by an external physical layer protocol (PHY) device.
mii_crs	I	113	Carrier sense is asserted by the PHY when the media is active.
mii_dv	I	111	Data valid is asserted by an external PHY when receive data is present on the **mii/sym_rxd** lines and is deasserted at the end of the packet. This signal should be synchronized with the **mii/sym_rclk** signal.
mii_err	I	110	Receive error asserts when a data decoding error is detected by an external PHY device. This signal is synchronized to **mii/sym_rclk** and can be asserted for a minimum of one receive clock. When asserted during a packet reception, it sets the cyclic redundancy check (CRC) error bit in the receive descriptor (RDES0).
mii_mdc	O	106	MII management data clock is sourced by the 21140A to the PHY devices as a timing reference for the transfer of information on the **mii_mdio** signal.

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Table 4 (Cont.) Functional Description of DECchip 21140A Signals

Signal	Type	Pin Number	Description
mii_mdio	I/O	105	MII management data input/output transfers control information and status between the PHY and the 21140A.
mii/srl	O	133	Indicates the selected port: SRL or MII/SYM. When asserted, the MII/SYM port is active. When deasserted, the SRL port is active.
mii/sym_rclk	I	114	Supports either the 25-MHz or 2.5-MHz receive clock. This clock is recovered by the PHY.
mii/sym_ rxd<3:0>	I	See Table 2.	Four parallel receive data lines when MII mode is selected. This data is driven by an external PHY that attached the media and should be synchronized with the **mii/sym_rclk** signal.
mii/sym_tclk	I	123	Supports the 25-MHz or 2.5-MHz transmit clock supplied by the external physical layer medium dependent (PMD) device. This clock should always be active.
mii/sym_ txd<3:0>	O	See Table 2.	Four parallel transmit data lines. This data is synchronized to the assertion of the **mii/sym_tclk** signal and is latched by the external PHY on the rising edge of the **mii/sym_tclk** signal.
mii/sym_txen	O	125	Transmit enable signals that the transmit is active to an external PHY device. This signal is ignored in PCS mode (CSR6<23>).
nc	O	104	No connection.
par	I/O	47	Parity is calculated by the 21140A as an even parity bit for the 32-bit **ad** and 4-bit **c_be_l** lines.
			During address and data phases, parity is calculated on all the **ad** and **c_be_l** lines whether or not any of these lines carry meaningful information.

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Table 4 (Cont.) Functional Description of DECchip 21140A Signals

Signal	Type	Pin Number	Description
pci_clk	I	5	The clock provides the timing for the 21140A related PCI bus transactions. All the bus signals are sampled on the rising edge of **pci_clk**. The clock frequency range is between 25 MHz and 33 MHz.
perr_l	I/O	45	Parity error asserts when a data parity error is detected. When the 21140A is the bus master and a parity error is detected, the 21140A asserts both CSR5 bit 13 (system error) and CFCS bit 8 (**serr_l** enable). Next, it completes the current data burst transaction, then stops operation. After the host clears the system error, the 21140A continues its operation. When the 21140A is the bus target and a parity error is detected, the 21140A asserts **perr_l**. This pin must be pulled up by an external resistor.
rcv_match	O	122	Receive match indication is asserted when a received packet has passed address recognition.
req_l	O	8	Bus request is asserted by the 21140A to indicate to the bus arbiter that it wants to use the bus.
rst_l	I	2	Resets the 21140A to its initial state. This signal must be asserted for at least 10 active PCI clock cycles. When in the reset state, all PCI output pins are put into tristate and all PCI O/D signals are floated.
sd	I	109	Signal detect indication supplied by an external physical layer medium dependent (PMD) device.

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Table 4 (Cont.) Functional Description of DECchip 21140A Signals

Signal	Type	Pin Number	Description
serr_l	I/O	46	If an address parity error is detected and CFCS bit 31 (detected parity error) is enabled, 21140A asserts both **serr_l** (system error) and CFCS bit 30 (signal system error). When an address parity error is detected, system error asserts two clocks after the failing address. This pin must be pulled up by an external resistor.
sr_ck	O	78	Serial ROM clock signal.
sr_cs	O	79	Serial ROM chip-select signal.
sr_di	O	77	Serial ROM data-in signal.
sr_do	I	76	Serial ROM data-out signal.
srl_clsn	I	134	Collision detect signals a collision occurrence on the Ethernet cable to the 21140A. It may be asserted and deasserted asynchronously by the external ENDEC to the receive clock.
srl_rclk	I	137	Receive clock carries the recovered receive clock supplied by an external ENDEC. During idle periods, **srl_rclk** may be inactive.
srl_rxd	I	135	Receive data carries the input receive data from the external ENDEC. The incoming data should be synchronous with the **srl_rclk** signal.
srl_rxen	I	136	Receive enable signals activity on the Ethernet cable to the 21140A. It is asserted when receive data is present on the Ethernet cable and is deasserted at the end of a frame. It may be asserted and deasserted asynchronously to the receive clock (**srl_rclk**) by the external ENDEC.
srl_tclk	I	139	Transmit clock carries the transmit clock supplied by an external ENDEC. This clock must always be active (even during reset).

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Table 4 (Cont.) Functional Description of DECchip 21140A Signals

Signal	Type	Pin Number	Description
srl_txd	O	138	Transmit data carries the serial output data from the 21140A. This data is synchronized to the **srl_tclk** signal.
srl_txen	O	140	Transmit enable signals an external ENDEC that the 21140A transmit is in progress.
stop_l	I/O	43	Stop indicator indicates that the current target is requesting the bus master to stop the current transaction. The 21140A responds to the assertion of **stop_l** when it is the bus master, either to disconnect, retry, or abort.
sym_link	O	124	Indicates that the descrambler is locked to the input data signal.
sym_rxd<4>	I	119	Receive data, together with the four receive lines **mii/sym_rxd<3:0>**, provide five parallel lines of data in symbol form for use in PCS mode (100BASE-T, CSR6<23>). This data is driven by an external PMD device and should be synchronized to the **mii/sym_rclk** signal.
sym_txd<4>	O	132	Transmit data, together with the four transmit lines **mii/sym_txd<3:0>**, provide five parallel lines of data in symbol form for use in PCS mode (100BASE-T, CSR6<23>). This data is synchronized on the rising edge of the **mii/sym_tclk** signal.
tck	I	141	JTAG clock shifts state information and test data into and out of the 21140A during JTAG test operations. This pin should not be left unconnected.
tdi	I	143	JTAG data in is used to serially shift test data and instructions into the 21140A during JTAG test operations. This pin should not be left unconnected.
tdo	O	144	JTAG data out is used to serially shift test data and instructions out of the 21140A during JTAG test operations.

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Table 4 (Cont.) Functional Description of DECchip 21140A Signals

Signal	Type	Pin Number	Description
tms	I	142	JTAG test mode select controls the state operation of JTAG testing in the 21140A. This pin should not be left unconnected.
trdy_l	I/O	41	Target ready indicates the target agent's ability to complete the current data phase of the transaction. A data phase is completed on any clock when both **trdy_l** and **irdy_l** are asserted. Wait cycles are inserted until both **irdy_l** and **trdy_l** are asserted together. When the 21140A is the bus master, target ready is asserted by the bus slave on the read operation, indicating that valid data is present on the **ad** lines. During a write cycle, it indicates that the target is prepared to accept data.
vdd	P	See Table 3.	3.3-V supply input voltage.
vdd_clamp	P	73	5.0-V reference for 5.0-V signaling environments and 3.3 V for 3.3-V signaling environments.
vss	P	See Table 3.	Ground pins.

2.2 Pin Tables

This section contains four types of pin tables:

- Table 5 lists the input pins.
- Table 6 lists the output pins.
- Table 7 lists the input/output pins.
- Table 8 lists the open drain pins.

Table 5 Input Pins

Signal	Active Level	Signal	Active Level
gnt_l	Low	**sd**	High
idsel	High	**sr_do**	High
mii_clsn	High	**srl_clsn**	High
mii_crs	High	**srl_rclk**	—
mii_dv	High	**srl_rxd**	—
mii_err	High	**srl_rxen**	High
mii/sym_rclk	—	**srl_tclk**	—
mii/sym_rxd<3:0>	—	**sym_rxd<4>**	—
mii/sym_tclk	—	**tck**	—
pci_clk	—	**tdi**	—
rst_l	Low	**tms**	High

Table 6 Output Pins

Signal	Active Level	Signal	Active Level
br_a<0>	High	**req_l**	Low
br_a<1>	High	**sr_ck**	—
br_ce_l	Low	**sr_cs**	High
mii_mdc	—	**sr_di**	High
mii/srl	—	**srl_txd**	—
mii/sym_txd<3:0>	—	**srl_txen**	High
mii/sym_txen	High	**sym_link**	High
nc	—	**sym_txd<4>**	—
rcv_match	High	**tdo**	High

Table 7 Input/Output Pins

Signal	Active Level	Signal	Active Level
ad<31:0>	—	**mii_mdio**	—
br_ad<7:0>	—	**par**	—
c_be_l<3:0>	Low	**perr_l**	Low
devsel_l	Low	**serr_l**	Low
frame_l	Low	**stop_l**	Low
gep<7:0>	—	**trdy_l**	Low
irdy_l	Low		

Table 8 Open Drain Pins

Signal	Active Level
int_l	Low

2.3 Signal Grouping by Function

Table 9 lists the signals according to their interface function.

Table 9 Signal Functions

Interface	Function	Signal
PCI	Address and data	**ad<31:0>**, **par**
	Arbitration	**gnt_l**, **req_l**
	Bus command and byte enable	**c_be_l<3:0>**
	Device select	**devsel_l**, **idsel**
	Error reporting	**perr_l**, **serr_l**
	Interrupt	**int_l**
	System	**pci_clk**, **rst_l**
	Control signals	**frame_l**, **stop_l**, **irdy_l**, **trdy_l**
MII/symbol	Transmit data lines	**mii/sym_txd<3:0>**
Network port	Receive data lines	**mii/sym_rxd<3:0>**
	Transmit, receive clocks	**mii/sym_tclk**, **mii/sym_rclk**
	SYM mode	**sym_rxd<4>**, **sym_txd<4>**
	Signal detection	**sd**
	Transmit enable	**mii/sym_txen**
	Collision detect	**mii_clsn**
	Error reporting	**mii_err**
	Data control	**mii_dv**, **mii_crs**
	MII management data clock	**mii_mdc**
	MII management data input/output	**mii_mdio**
Serial network port	Transmit and receive data	**srl_txd**, **srl_rxd**
	Transmit control	**srl_txen**, **srl_tclk**
	Receive control	**srl_rxen**, **srl_rclk**
	Collision detect	**srl_clsn**

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Table 9 (Cont.) Signal Functions

Interface	Function	Signal
Miscellaneous	LED indicators	**rcv_match**, **sym_link**
	General-purpose pins	**gep<7:0>**
	MII/SYM and serial port select	**mii/srl**
Test access port	JTAG test operations	**tck**, **tdi**, **tdo**, **tms**
Serial ROM port	Serial ROM	**sr_ck**, **sr_cs**, **sr_di**, **sr_do**
Boot ROM	ROM interface	**br_a<1:0>**, **br_ad<7:0>**, **br_ce_l**
Power	3.3-V and 5.0-V supply input	**vdd**, **vdd_clamp**
	Ground	**vss**

3 Electrical and Environmental Specifications

This section contains the electrical and environmental specifications for the 21140A.

Caution

Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21140A. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21140A.

3.1 Voltage Limit Ratings

Table 10 lists the voltage limit ratings.

Table 10 Voltage Limit Ratings

Parameter	Minimum	Maximum
Power supply voltage	+3.0 V	+3.6 V
vdd_clamp (3.3 V)	+3.0 V	+3.6 V
vdd_clamp (5.0 V)	+4.75 V	+5.25 V
ESD protection voltage	—	2000 V

3.2 Temperature Limit Ratings

Table 11 lists the temperature limit ratings.

Table 11 Temperature Limit Ratings

Parameter	Minimum	Maximum
Storage temperature	–55°C	+125°C
Operating temperature	0°C	70°C

3.3 Supply Current and Power Dissipation

The values in Table 12 are estimates based on a PCI clock frequency of 33 MHz and a network data rate of 10Mb/s for SRL and 10/100Mb/s for MII.

Table 12 Supply Current and Power Dissipation

Symbol	Conditions	Typical	Maximum	Units
IDD	**vdd** = 3.6 V, Ta = 70°C	135	190	mA
Normal power mode	**vdd** = 3.6 V, Ta = 70°C	0.48	0.68	W
Snooze power mode	**vdd** = 3.6 V, Ta = 70°C	0.28	0.36	W
Sleep power mode	**vdd** = 3.6 V, Ta = 70°C	0.21	0.28	W

3.3.1 PCI I/O Voltage Specifications

The 21140A meets the I/O voltage specifications listed in Table 13 and Table 14.

Table 13 I/O Voltage Specifications for 5.0-V Levels

Symbol	Parameter	Condition	Minimum	Maximum
V_{ih}	Input high voltage	—	2.0 V	**vdd_clamp** + 0.5 V
V_{il}	Input low voltage	—	–0.5 V	0.8 V
I_i[1]	Input leakage current	0.5 V < V_{in} < 2.7 V	—	±70 µA
V_{oh}	Output high voltage	I_{out} = –2 mA	2.4 V	—
V_{ol}[2]	Output low voltage	I_{out} = 3 mA, 6 mA	—	0.55 V
Cap[3]	Pin capacitance	—	5 pF	8 pF

[1]Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.

[2]Signals without pull-up resistors have a low output current of 3 mA. Signals requiring pull-up resistors (including **frame_l, trdy_l, irdy_l, devsel_l, stop_l, serr_l,** and **perr_l**) have a low output current of 6 mA.

[3]Parameter design guarantee.

Table 14 I/O Voltage Specifications for 3.3-V Levels

Symbol	Parameter	Condition	Minimum	Maximum
V_{ih}	Input high voltage	—	0.475 ∗ **vdd_clamp**	**vdd_clamp** + 0.5 V
V_{il}	Input low voltage	—	–0.5 V	0.325 ∗ **vdd_clamp**
I_i[1]	Input leakage current	0.0 V < V_{in} < **vdd_clamp**	—	±70 µA
V_{oh}	Output high voltage	I_{out} = –500 µA	0.9 ∗ **vdd_clamp**	—
V_{ol}	Output low voltage	I_{out} = 1500 µA	—	0.1 ∗ **vdd_clamp**
Cap[2]	Pin capacitance	—	5 pF	8 pF

[1]Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.

[2]Parameter design guarantee.

3.3.2 PCI Reset

PCI reset (**pci_rst**) is an asynchronous signal that must be active for at least 10 active PCI clock (**pci_clk**) cycles. Figure 3 shows the PCI reset timing characteristics, and Table 15 lists the PCI reset signal limits.

Figure 3 PCI Reset Timing Diagram

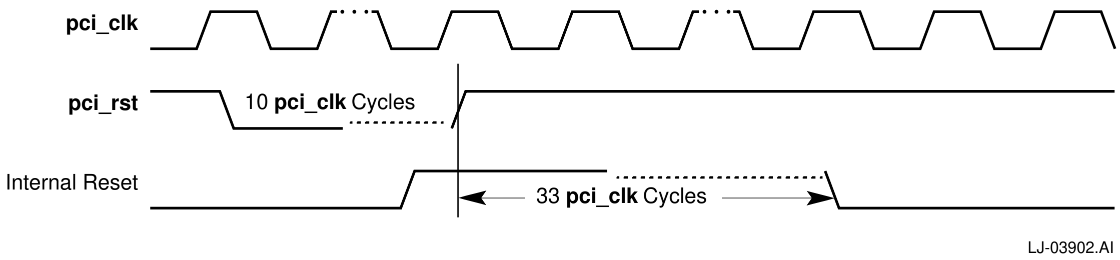


Table 15 PCI Reset Timing

Symbol	Parameter	Minimum	Maximum	Conditions
Trst	**pci_rst** pulse width	10 ∗ Tcycle	Not applicable	**pci_clk** active

3.3.3 PCI Clock Specifications

The clock frequency range for the PCI is between 20 MHz and 33 MHz.[4] Figure 4 shows the PCI clock specification timing characteristics, and Table 16 lists the frequency-derived clock specifications.

Figure 4 PCI Clock Specifications Timing Diagram

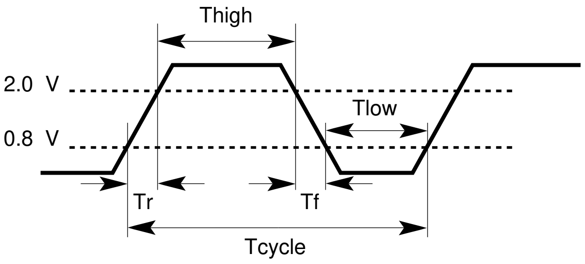


Table 16 PCI Clock Specifications

Symbol	Parameter	Minimum	Maximum	Notes
Tcycle	Cycle time	30 ns	50 ns	—-
Thigh	**pci_clk** high time	12 ns	—-	At 2 V
Tlow	**pci_clk** low time	12 ns	—-	At 0.8 V
Tr/Tf[1]	**pci_clk** slew rate	1 V/ns	4 V/ns	—-

[1]Rise and fall times are specified in terms of the edge rate measured in V/ns. Parameter design guarantee.

[4] The PCI clock frequency is from dc to 33 MHz; network operational with the PCI clock from 20 MHz to 33 MHz.

3.3.4 Other PCI Signals

Figure 5 shows the timing diagram characteristics, and Table 17 lists the other PCI signals. This timing is identical to the timing for the general-purpose register signals.

Figure 5 Timing Diagram for Other PCI Signals

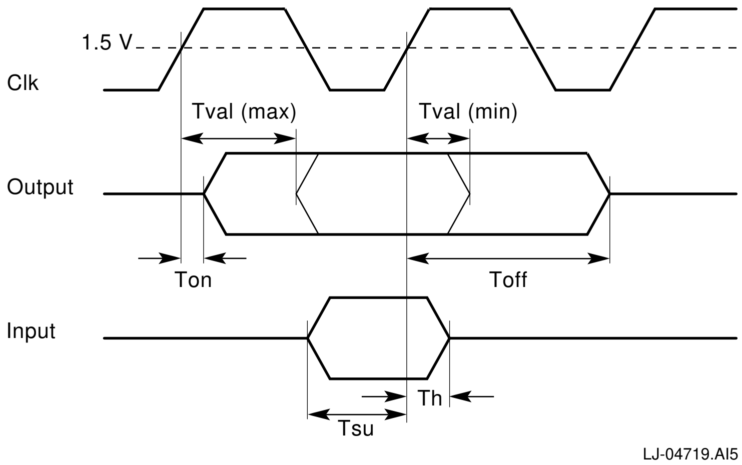


Table 17 Other PCI Signals

Symbol	Parameter	Minimum	Maximum	Conditions
Tval	clk-to-signal valid delay	2 ns	11 ns	Cload = 50 pF
Ton[1]	Float-to-active delay from clk	2 ns	—	—
Toff[1]	Active-to-float delay from clk	—	28 ns	—
Tsu	Input signal valid setup time before clk	7 ns	—	—
Th	Input signal hold time from clk	0 ns	—	—
Tr[1]	Unloaded output rise time	—	2 ns	0.4 V to 2.4 V
Tf[1]	Unloaded output fall time	—	2 ns	2.4 V to 0.4 V

[1]Parameter design guarantee

3.4 Serial, MII/SYM, Boot ROM, Serial ROM, and General-Purpose Port Interface Specifications

Table 18 lists the specifications for the serial, MII/SYM, boot ROM, serial ROM, and general-purpose port interfaces.

Table 18 Serial, MII/SYM, Boot ROM, Serial ROM, and General-Purpose Port

Symbol	Definition	Condition	Minimum	Maximum	Units
V_{oh}	Output high voltage	I_{oh} = –4 mA	2.4	—	V
V_{ol}	Output low voltage	I_{ol} = 4 mA	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_{in}	Input current	$V_{in} = V_{cc}$ or V_{ss}	–10.0	10.0	µA
I_{oz}[1]	Maximum tristate output leakage current	$V_{in} = V_{dd}$ or V_{ss}	–10.0	10.0	µA

[1]For **sr_do** and **br_ce_l** the maximum value is 1000.0 µA.

3.5 Serial Network Port Timing

This section describes the serial network port timing limits.

3.5.1 Serial 10Mb/s Timing—Transmit

Figure 6 shows the serial network port transmit timing characteristics, and Table 19 lists the serial network port transmit timing limits.

Figure 6 Serial Network Port Timing Diagram—Transmit

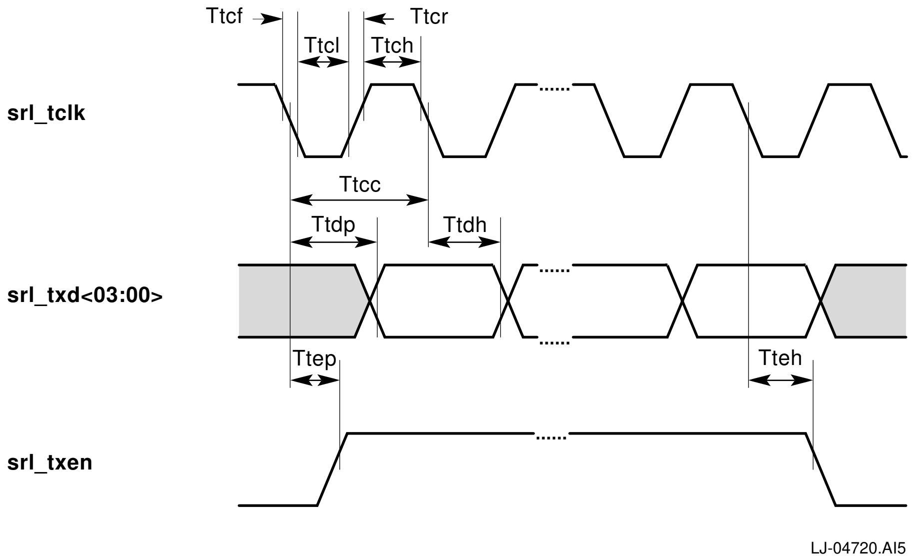


Table 19 Serial Network Port Timing—Transmit

Symbol	Definition	Minimum	Maximum	Units
Ttcl	**srl_tclk** low time	45	55	ns
Ttch	**srl_tclk** high time	45	55	ns
Ttcr[1]	**srl_tclk** rise time	—	8	ns
Ttcf[1]	**srl_tclk** fall time	—	8	ns
Ttdp	**srl_tclk** fall time to **srl_txd** valid	—	26	ns
Ttdh	**srl_txd** hold after **srl_tclk** fall time	5	—	ns
Ttep	**srl_tclk** fall time to **srl_txen** valid	—	26	ns
Tteh	**srl_txen** hold after **srl_tclk** fall time	5	—	ns

[1]Parameter design guarantee

3.5.2 Serial 10Mb/s Timing—Collision

Figure 7 shows the serial network port collision timing characteristics, and Table 20 lists the serial network port collision timing limit.

Figure 7 Serial Network Port Timing Diagram—Collision

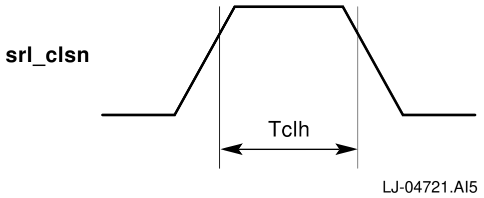


Table 20 Serial Network Port Timing—Collision

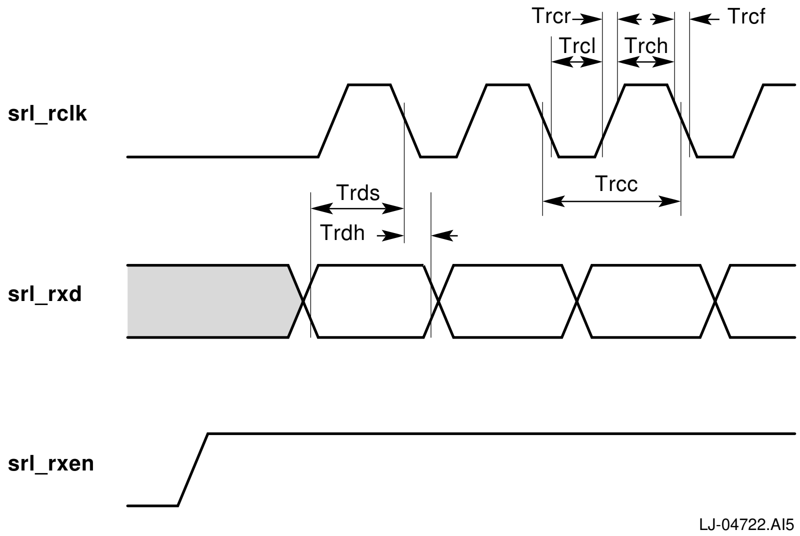
Symbol	Definition	Minimum	Maximum	Units
Tclh[1]	**srl_clsn** high time	20	—	ns

[1]Parameter design guarantee

3.5.3 Serial 10Mb/s Timing—Receive, Start of Packet

Figure 8 shows the serial network port timing characteristics in receive mode, start of packet; and Table 21 lists the serial network port timing limits in receive mode, start of packet.

Figure 8 Serial Network Port Timing Diagram—Receive, Start of Packet



3.5.4 Serial 10Mb/s Timing—Receive, End of Packet

Figure 9 shows the serial network port timing characteristics in receive mode, end of packet; and Table 21 lists the serial network port timing limits in receive mode, end of packet.

Figure 9 Serial Network Port Timing Diagram—Receive, End of Packet

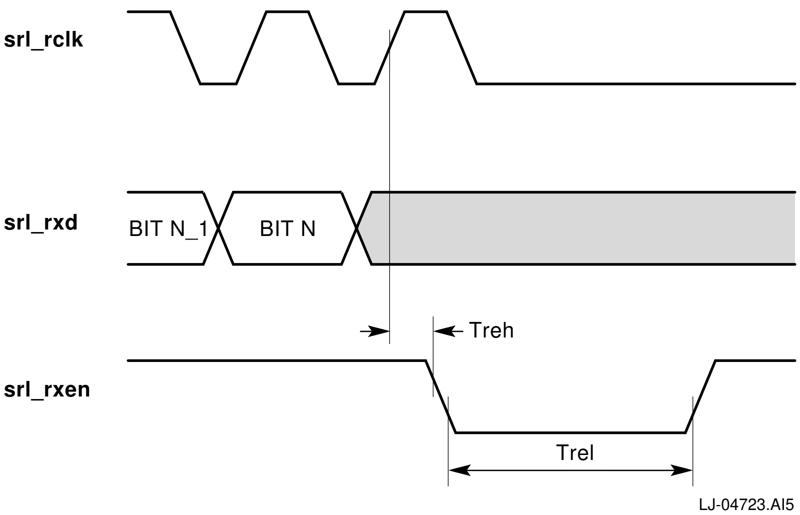


Table 21 Serial Network Port Timing—Receive, Start, and End of Packet

Symbol	Definition	Minimum	Maximum	Units
Trcc	**srl_rclk** cycle time	85	118	ns
Trcl	**srl_rclk** low time	38	80	ns
Trch	**srl_rclk** high time	38	80	ns
Trcr[1]	**srl_rclk** rise time	—	8	ns
Trcf[1]	**srl_rclk** fall time	—	8	ns
Trds	**srl_rxd** setup to **srl_rclk** fall time	10	—	ns
Trdh	**srl_rxd** hold after **srl_rclk** fall time	5	—	ns
Trel	**srl_rxen** low time	120	—	ns
Treh	**srl_rxen** hold after **srl_rclk** rise time	10	100	ns

[1]Parameter design guarantee

3.6 MII/SYM Port Timing

This section describes the MII/SYM port timing limits.

3.6.1 MII/SYM 10/100Mb/s and 10Mb/s Timing—Transmit

Figure 10 shows the MII/SYM port transmit timing characteristics, and Table 22 lists the MII/SYM port transmit timing limits.

Figure 10 MII/SYM Port Timing Diagram—Transmit

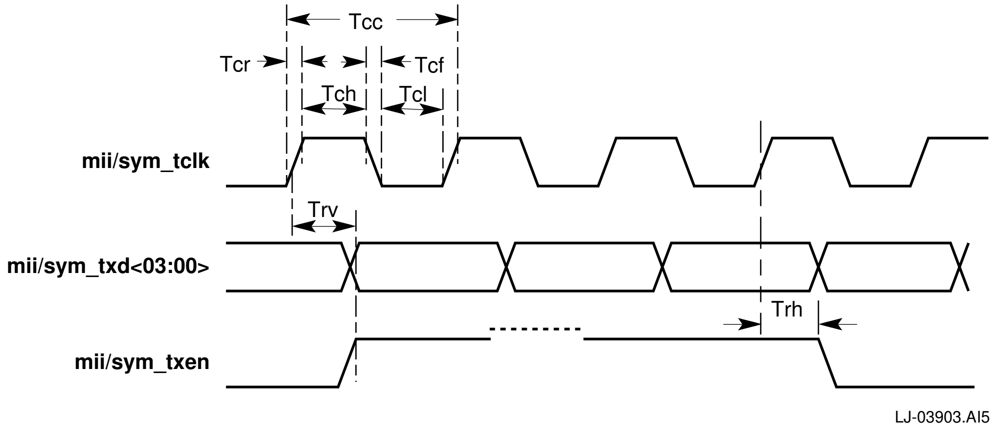


Table 22 MII/SYM Port Timing—Transmit

Symbol	Definition	Minimum	Typical	Maximum	Units
Tcc[1,2]	**mii/sym_tclk** cycle time	—	40t	—	ns
Tch[2]	**mii/sym_tclk** high time	10t	—	26t	ns
Tcl[2]	**mii/sym_tclk** low time	10t	—	26t	ns
Tcr	**mii/sym_tclk** rise time	—	8	—	ns
Tcf	**mii/sym_tclk** fall time	—	8	—	ns
Trv[3]	**mii/sym_tclk** rise to **mii/sym_txen** valid time or **mii/sym_tclk** rise to **mii/sym_txd** valid time	—	—	20	ns
Trh	**mii/sym_txen** hold after **mii/sym_tclk** rise time	5	—	—	ns

[1] ±50 parts per million.

[2] t = 1 for 100Mb/s operation and t = 10 for 10Mb/s operation.

[3] Outputs transmit data (**mii/sym_txd**) and transmit enable (**mii/sym_txen**) are driven internally from the rising edge of **mii/sym_tclk**.

3.6.2 MII/SYM 10/100Mb/s Timing—Receive

Figure 11 shows the MII/SYM port receive timing characteristics, and Table 23 lists the MII/SYM port receive timing limits.

Figure 11 MII/SYM Port Timing Diagram—Receive

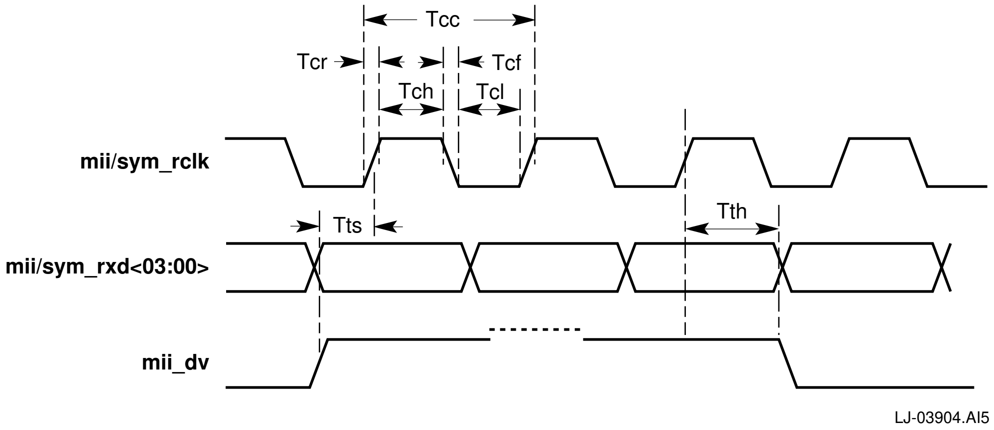


Table 23 MII/SYM Port Timing—Receive

Symbol	Definition	Minimum	Typical	Maximum	Units
Tcc[1,2]	**mii/sym_rclk** cycle time	—	40t	—	ns
Tch[2]	**mii/sym_rclk** high time	14t	—	26t	ns
Tcl[2]	**mii/sym_rclk** low time	14t	—	26t	ns
Tcr	**mii/sym_rclk** rise time	—	8	—	ns
Tcf	**mii/sym_rclk** fall time	—	8	—	ns
Tts[3]	**mii/sym_rxd** setup (both rise and fall transactions) to **mii/sym_rclk** rise time or **mii_dv** setup (both rise and fall transactions) to **mii/sym_rclk** rise time	6	—	—	ns
Tth	**mii/sym_rxd** hold (both rise and fall transactions) after **mii/sym_rclk** rise time or **mii_dv** hold (both rise and fall transactions) after **mii/sym_rclk** rise time	10	—	—	ns

[1] ±50 parts per million.

[2] t = 1 for 100Mb/s operation and t = 10 for 10Mb/s operation.

[3] Inputs receive data (**mii/sym_rxd**) and data valid (**mii_dv**) are latched internally on the rising edge of **mii/sym_rclk**.

3.6.3 MII/SYM 10/100Mb/s Timing—Signal Detect

Figure 12 shows the MII/SYM port signal detect timing characteristics, and Table 24 lists the MII/SYM port signal detect timing limits.

Figure 12 MII/SYM Port Timing Diagram—Signal Detect

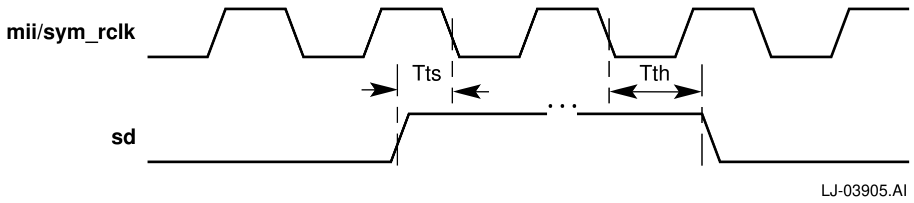


Table 24 MII/SYM Port Timing—Signal Detect

Symbol	Definition	Minimum	Maximum	Units
Tts[1]	**sd** setup (both rise and fall transactions) to **mii/sym_rclk** fall time	10	—	ns
Tth[1]	**sd** hold (both rise and fall transactions) after **mii/sym_rclk** fall time	12	—	ns

[1]Input signal detect (**sd**) is latched internally on the falling edge of **mii/sym_rclk**.

3.6.4 MII/SYM 10/100Mb/s Timing—Receive Error

Figure 13 shows the MII/SYM port receive error timing characteristics, and Table 25 lists the MII/SYM port receive error timing limits.

Figure 13 MII/SYM Port Timing Diagram—Receive Error

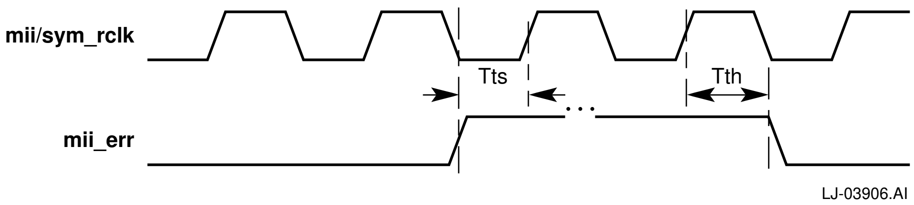


Table 25 MII/SYM Port Timing—Receive Error

Symbol	Definition	Minimum	Maximum	Units
Tts[1]	**mii_err** setup (both rise and fall transactions) to **mii/sym_rclk** rise time	10	—	ns
Tth[1]	**mii_err** hold (both rise and fall transactions) after **mii/sym_rclk** rise time	10	—	ns

[1]Input receive error (**mii_err**) is latched internally on the rising edge of **mii/sym_rclk**.

3.6.5 MII/SYM 10/100Mb/s Timing—Carrier Sense and Collision

Figure 14 shows the MII/SYM port carrier sense and collision timing characteristics, and Table 26 lists the MII/SYM port carrier sense and collision timing limits.

Figure 14 MII/SYM Port Timing Diagram—Carrier Sense and Collision

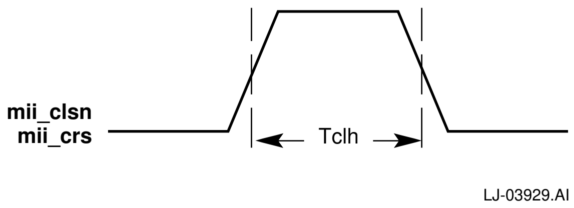


Table 26 MII/SYM Port Timing—Carrier Sense and Collision

Symbol	Definition	Minimum	Maximum	Units
Tclh	**mii_crs**, **mii_clsn** high time	20	—	ns

3.7 Boot ROM Port Timing

This section describes the boot ROM port timing.

3.7.1 Boot ROM Read Timing

Figure 15 shows the boot ROM read timing characteristics, and Table 27 lists the boot ROM read timing limits.

Figure 15 Boot ROM Read Timing Diagram

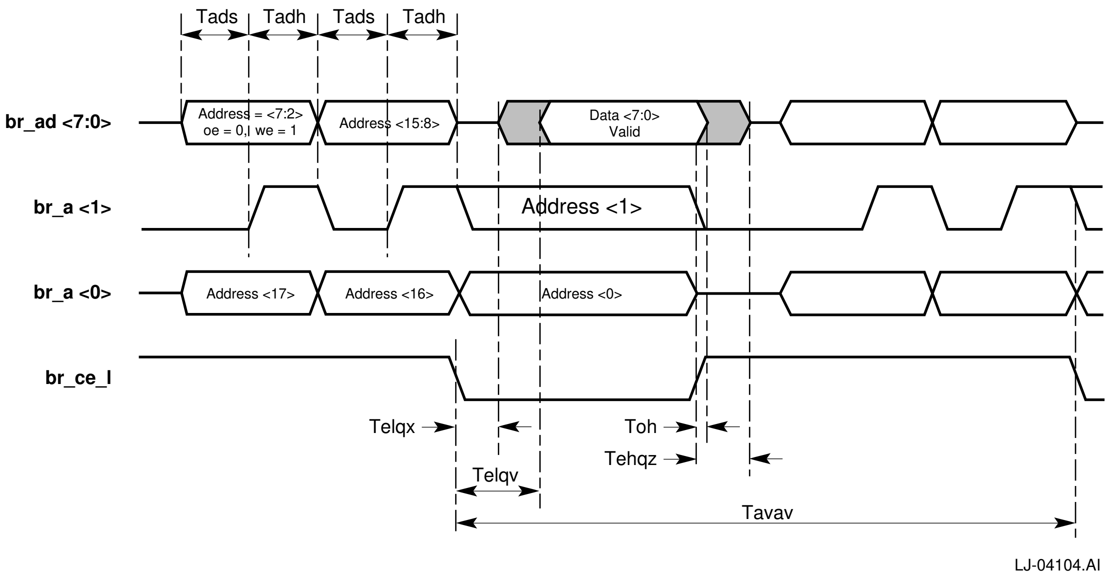


Table 27 Boot ROM Read Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Tavav	Read cycle time	120	—	ns
Telqv	**br_ce_l** to output delay	—	120	ns
Telqx[1]	**br_ce_l** to output enable	0	—	ns
Tehqz[1]	**br_ce_l** rising edge to output high impedance	—	55	ns
Toh	Output hold from **br_ce_l** change	0	—	ns
Tads	Address setup to latch enable high	30	—	ns
Tadh	Address hold from latch enable high	30	—	ns

[1]Parameter design guarantee

3.7.2 Boot ROM Write Timing

Figure 16 shows the boot ROM write timing characteristics, and Table 28 lists the boot ROM write timing limits.

Figure 16 Boot ROM Write Timing Diagram

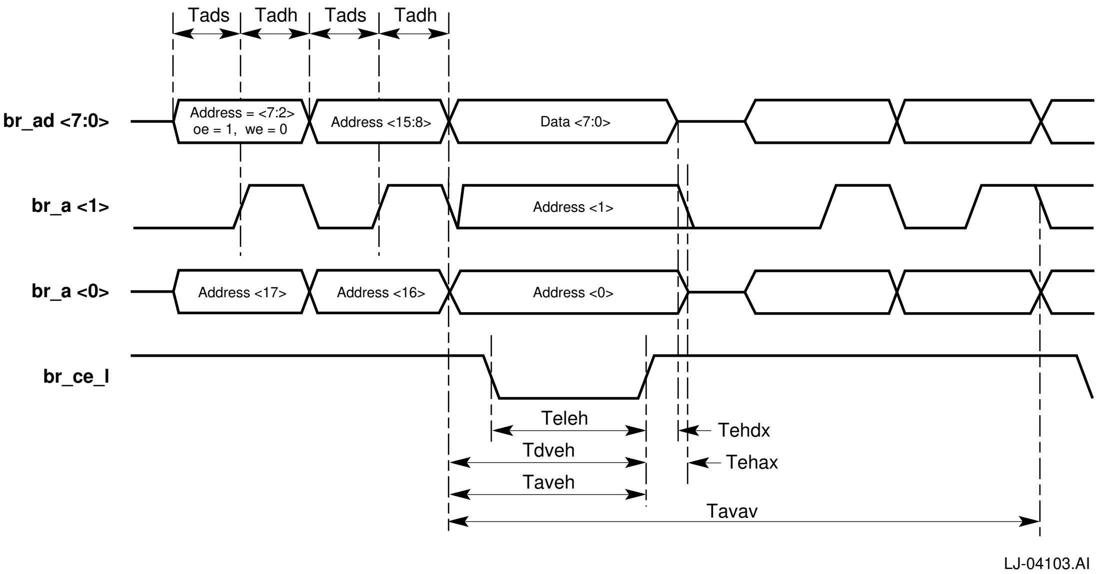


Table 28 Boot ROM Write Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Tavav	Write cycle time	120	—	ns
Teleh	**br_ce_l** pulse width	70	—	ns
Taveh	Address setup to **br_ce_l** rising edge	50	—	ns
Tdveh	Data setup to **br_ce_l** rising edge	50	—	ns
Tehdx	Data hold from **br_ce_l** rising edge	10	—	ns
Tehax	Address hold from **br_ce_l** high	15	—	ns
Tads	Address setup to latch enable high	30	—	ns
Tadh	Address hold from latch enable high	30	—	ns

3.8 Serial ROM Port Timing

Figure 17 shows the serial ROM port timing, and Table 29 lists the characteristics. This timing is identical to the timing for the MII management signals (**mii_mdio** and **mii_mdc**).

Figure 17 Serial ROM Port Timing Diagram

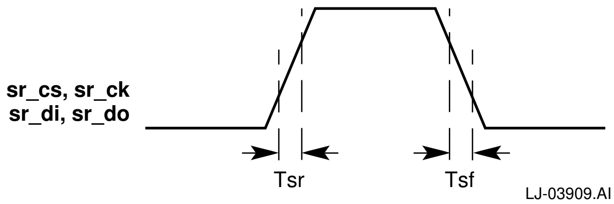


Table 29 Serial ROM Port Timing Characteristics

Symbol	Definition	Minimum	Maximum	Units
Tsr[1]	Rise time	—	10	ns
Tsf[1]	Fall time	—	10	ns

[1]Parameter design guarantee

3.9 External Register Timing

Figure 18 shows the external register read timing characteristics, and Figure 19 shows its write timing characteristics. Table 30 lists the external register timing specifications for both read and write operations.

Figure 18 External Register Read Timing Diagram

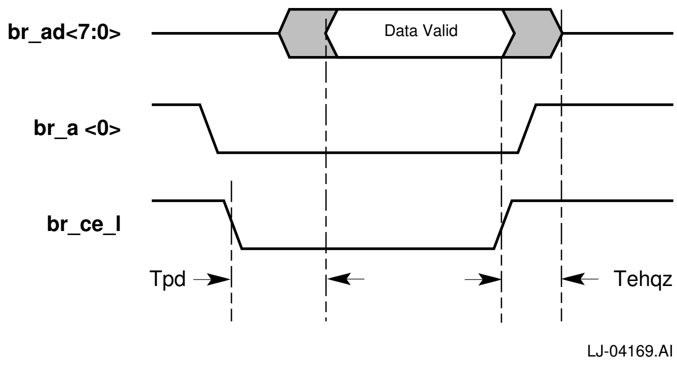


Figure 19 External Register Write Timing Diagram

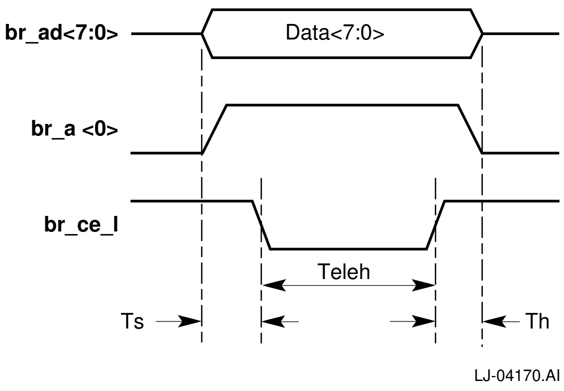


Table 30 External Register Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Teleh	**br_ce_l** pulse width	120	—	ns
Read Timing				
Tpd	**br_ce_l** low to **br_ad<7:0>** valid	—	20	ns
Tehqz[1]	**br_ce_l** high to **br_ad<7:0>** high impedance	—	20	ns
Write Timing				
Ts	Data setup time prior to **br_ce_l**	30	—	ns
Th	Data hold after **br_ce_l** high	30	—	ns

[1]Parameter design guarantee

3.10 Joint Test Action Group—Test Access Port

This section provides the joint test action group (JTAG) test access port specifications.

3.10.1 JTAG dc Specifications

Table 31 lists the dc specifications for the JTAG pins.

Table 31 JTAG dc Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
V_{oh}	Output high voltage	I_{oh} = –4 mA	2.4	—	V
V_{ol}	Output low voltage	I_{ol} = 4 mA	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_{ip}	Input leakage current on pins with internal pull-up resistors (**tdi**, **tms**, and **tck**)	0.0 <Vin<**vdd**	—	+20/–1000[1]	μA
I_{oz}	Tristate output leakage current (**tdo**)	0.0 <Vout<**vdd**	—	±20	μA

[1]For **tdi**, **tms**, and **tck** pins that have internal pull-up resistors, the maximum leakage current of 1 mA can occur when Vin = 0 V.

3.10.2 JTAG Boundary-Scan Timing

Figure 20 shows the JTAG boundary-scan timing, and Table 32 lists the interface signal timing relationships.

Figure 20 JTAG Boundary-Scan Timing Diagram

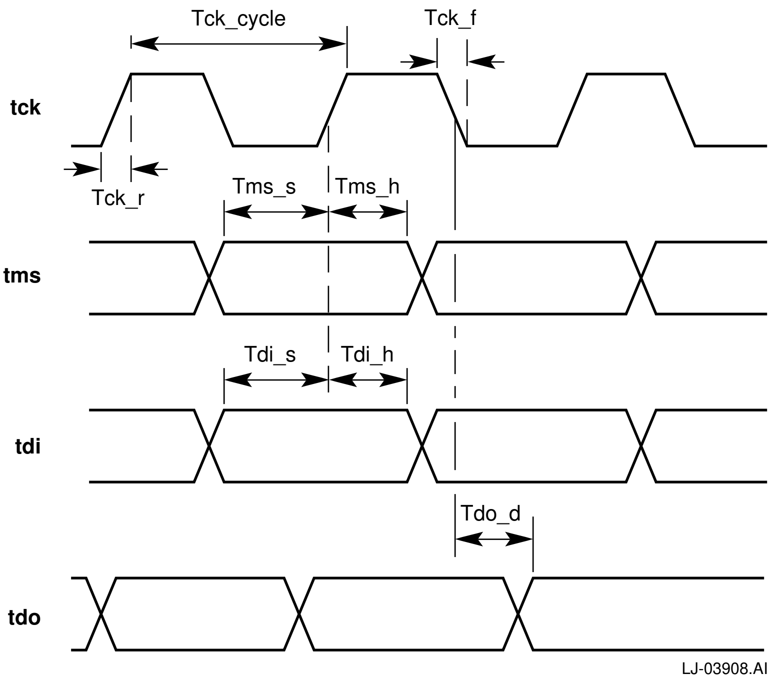


Table 32 JTAG Interface Signal Timing Relationships

Symbol	Parameter	Minimum	Maximum	Units
Tms_s	**tms** setup time	20	—	ns
Tms_h	**tms** hold time	5	—	ns
Tdi_s	**tdi** setup time	20	—	ns
Tdi_h	**tdi** hold time	5	—	ns
Tdo_d	**tdo** delay time	—	20	ns
Tck_r[1]	**tck** rise time	—	3	ns
Tck_f[1]	**tck** fall time	—	3	ns
Tck_cycle	**tck** cycle time	90	—	ns

[1]Parameter design guarantee

4 Mechanical Specifications

The 21140A is contained in a 144-pin PQFP. Table 33 lists the mechanical specifications, and Figure 21 shows the mechanical layout of the 21140A.

Note

The basic (BSC) value in Table 33 is the default tolerance.

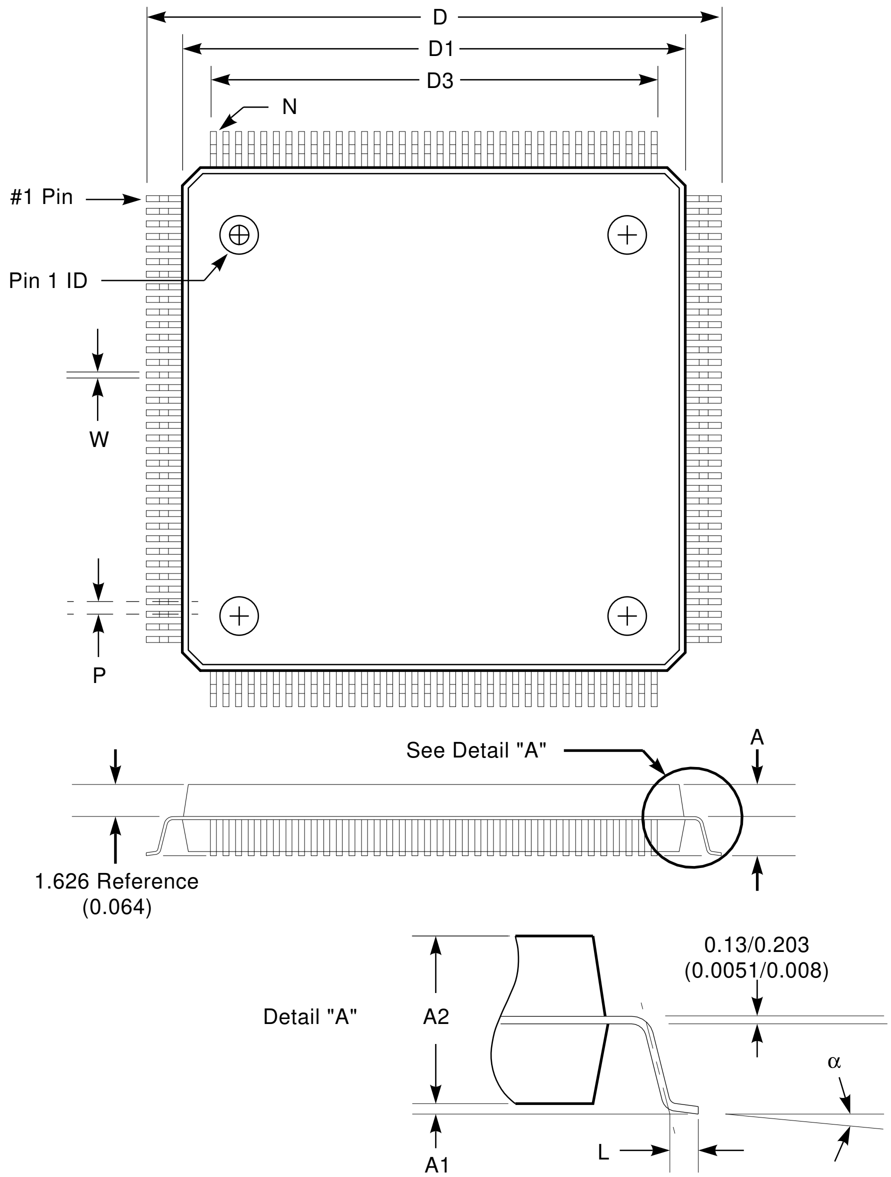
A value between 0 to 5 is ±0.1
A value between 5 to 30 is ±0.2
A value between 30 to 100 is ±0.3

Table 33 Mechanical Specifications

Item	Minimum[1]	Nominal[1]	Maximum[1]
A	—	—	4.07
A1	0.25	—	—
A2	3.17	3.37	3.67
D	—	31.20 BSC	—
D1	—	28.00 BSC	—
D3	—	22.75 reference	—
L	0.65	0.80	1.00
N	—	144	—
P	—	0.65 BSC	—
W	0.22	0.30	0.38
α	0°	—	7°

[1] All dimensions (except α) are in millimeters.

Figure 21 Mechanical Layout of the DECchip 21140A



Note: All dimensions (except α) are in millimeters.

LJ-04510.AI5

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To order the DECchip 21140A PCI Fast Ethernet LAN Controller and evaluation board, contact your local distributor.

You can order the following semiconductor products from Digital:

Product	Order Number
DECchip PCI 21140A Fast Ethernet LAN Controller	21140–AC
DECchip 21140A Evaluation Board Kit	21A40–04

Ordering Associated Literature

The following table lists some of the available Digital Semiconductor literature. For a complete list, contact the Digital Semiconductor Information Line.

Title	Order Number
DECchip 21140A PCI Fast Ethernet LAN Controller Product Brief	EC–QN7MA–TE
DECchip 21140A PCI Fast Ethernet LAN Controller Hardware Reference Manual	EC–QN7NB–TE
Using the DECchip 21140A with Boot ROM, Serial ROM and External Register: An Application Note	EC–QPQWA–TE

Ordering Third-Party Literature

You can order the following third-party literature directly from the vendor:

Title	Vendor
PCI Local Bus Specification Revision 2.1 PCI BIOS Specification Revision 2.1	PCI Special Interest Group 1–800–433–5177 (U.S.) 1–503–797–4207 (International) 1–503–234–6762 (FAX)