EC–QD2RA–TE

DECchip 21064 and DECchip 21064A Alpha AXP Microprocessors Hardware Reference Manual Update

This document provides updated information for the *DECchip 21064 and DECchip 21064A Alpha AXP Microprocessors Hardware Reference Manual*, EC–Q9ZUA–TE.

Add the following item to the list on page xxv.

- FDIV F/S and FDIV G/T in Section 2.10.2

Add the following paragraph to the bottom of page 2-27 in Section 2.10.2, **Producer-Consumer Latency**.

The **21064A** includes floating-point divide hardware that implements a non-restoring, normalizing, variable-shift algorithm. The algorithm retires an average of 2.4 bits per cycle. The typical divide latency, including pipeline overhead, will be 29/25 cycles for double precision operations and 19/15 cycles for single precision operations. The worst-case values for the **21064A** operations are the same as the **21064** (63/59 and 34/30), as shown in Figure 2-8.

The following table replaces Table 4-7, **Internal Processor Register Access**.

Mnemonic	PAL	ABX	IBX	INDEX	Access	Comments
TB_TAG	x	x	1	0	W	PALmode only
ITB_PTE	x	x	1	1	R/W	PALmode only
ICCSR	x	x	1	2	R/W	
ITB_PTE_TEMP	x	x	1	3	R	PALmode only
EXC_ADDR	x	x	1	4	R/W	
SL_RCV	x	x	1	5	R	
ITBZAP	x	x	1	6	W	PALmode only
ITBASM	x	x	1	7	W	PALmode only
ITBIS	x	x	1	8	W	PALmode only
PS	x	x	1	9	R/W	
EXC_SUM	x	x	1	10	R/W	
PAL_BASE	x	x	1	11	R/W	
HIRR	x	x	1	12	R	
SIRR	x	x	1	13	R/W	
ASTRR	x	x	1	14	R/W	
HIER	x	x	1	16	R/W	
SIER	x	x	1	17	R/W	
ASTER	x	x	1	18	R/W	
SL_CLR	x	x	1	19	W	
SL_XMIT	x	x	1	22	W	
TB_CTL	x	1	x	0	W	
DTB_PTE	x	1	x	2	R/W	
DTB_PTE_TEMP	x	1	x	3	R	
MM_CSR	x	1	x	4	R	
VA	x	1	x	5	R	
DTBZAP	x	1	x	6	W	
DTBASM	x	1	x	7	W	
DTBIS	x	1	x	8	W	
BIU_ADDR	x	1	x	9	R	
BIU_STAT	x	1	x	10	R	

Mnemonic	PAL	ABX	IBX	INDEX	Access	Comments
C_STAT	x	1	x	12	R	**21064A** only
DC_STAT	x	1	x	12	R	**21064** only
FILL_ADDR	x	1	x	13	R	
ABOX_CTL	x	1	x	14	W	
ALT_MODE	x	1	x	15	W	
CC	x	1	x	16	W	
CC_CTL	x	1	x	17	W	
BIU_CTL	x	1	x	18	W	
FILL_SYNDROME	x	1	x	19	R	
BC_TAG	x	1	x	20	R	
FLUSH_IC	x	1	x	21	W	
FLUSH_IC_ASM	x	1	x	23	W	
PAL_TEMP [31..0]	1	x	x	31-00	R/W	

The following text replaces Section 6.6.5.2, **Icache Parity Errors—21064A Only**.

Icache parity errors encountered while the **21064A** is executing native mode instructions are recoverable. In the event of an Icache parity error, the **21064A** will set C_STAT[IC_ERR] and will initiate a machine check if enabled by ABOX_CTL[MCHK_EN]. When the **21064A** performs any machine check, regardless of cause, it flushes the Icache. PALcode can log the error and return to executing native mode instructions.

Icache parity errors encountered while the **21064A** is executing PALcode available from Digital are not recoverable. PALcode available from Digital does not protect the EXC_ADDR register from being written (over the return address) if a machine check exception occurs.

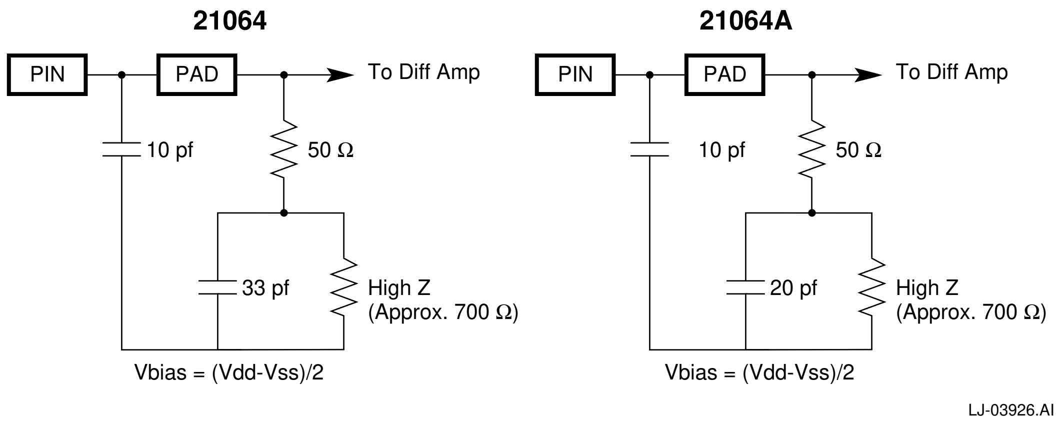
Some Icache parity errors encountered while the **21064A** is executing custom PALcode, written by the user with the help of Digital, could be recoverable. The return address in the EXC_ADDR register should be saved soon after entering any PALcode routine. You must measure degraded performance of the custom PALcode routine against the increased level of protection from nonrecoverable Icache parity errors. Protection cannot be absolute because instructions up to and including the instruction that saves the return address in the EXC_ADDR register are exposed to nonrecoverable parity errors.

The following table replaces Table 7-2, **dc Input/Output Characteristics**.

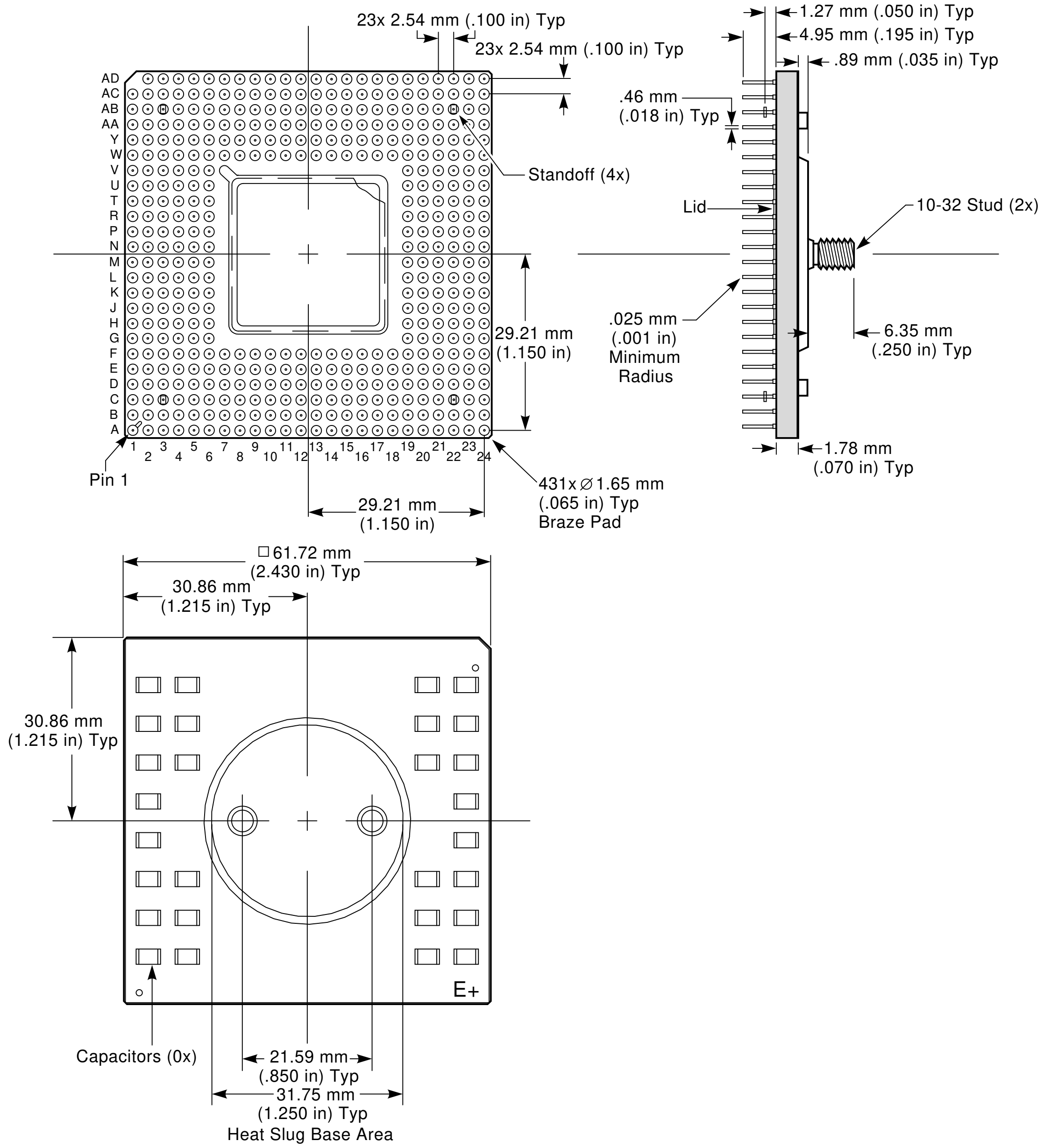
Symbol	Description	Min	Max	Units	Test Conditions
Vdd	Power supply voltage	3.135	3.465	V	–
Vih	High-level input voltage (except dcOk_h and cont_l)	2.0	–	V	–
Vihs	High-level input voltage (static pins dcOk_h and cont_l)	2.7	–	V	–
Vil	Low-level input voltage	–	0.8	V	–
Voh	High-level output voltage Ioh = 100 μA	2.4	–	V	–
Vol	Low-level output voltage Iol = 3.2 mA	–	0.4	V	–
Vdiffc	Differential clock input swing (duty cycle 45–55%)	300 mV	3.0	V	–
Iil	Input leakage current (except eclOut_h)	–100	100	μA	0<Vin<Vdd V
Iel	Input leakage current (eclOut_h)	–150	150	μA	0<Vin<Vdd V
Ioz	Output leakage current (tristate)	–100	100	μA	–
Icin	Clock input leakage	–4	4	mA	0<Vin<3.465 V

Note: Values in this table are valid only for Vref = 1.4 V.

The following figure replaces Figure 7-1, **Clock Termination**.



The following figure replaces Figure 10-1, **21064 Package Dimensions**.



The following figure replaces Figure 10-2, **21064A Package Dimensions**. The two differences from Figure 10-1 are the label E45 and Capacitors (14x).