EC–QD2MA–TE

DECchip 21041 DC1017-BA Errata
Revision 1.0
27-Apr-1995

Congratulations on your purchase of the DECchip 21041 PCI Ethernet LAN Controller chip or evaluation board containing the DECchip 21041. This document contains errata for the DECchip 21041 PCI Ethernet LAN Controller (revision DC1017-BA). It describes the following anomalies associated with this chip and offers workarounds that allow system designers and driver developers to use the DECchip 21041 successfully:

- Receive Watchdog Interrupt
- Capture-Effect Algorithm
- Auto-Negotiation Support
- Underflow Reporting

Receive Watchdog Interrupt

Background

The DECchip 21041 watchdog timer monitors the time that has elapsed since the beginning of each incoming packet. If the watchdog timer expires before a packet ends, the following events occur:

- The reception of the packet is halted.
- RDES0<4> (RJ-Receive Watchdog) and RDES0<8> (LS-Last Descriptor) are asserted in the current receive descriptor, then the descriptor is closed.
- CSR5<9> (RWT-Receive Watchdog Timeout) and CSR5<6> (RI-Receive Interrupt) are asserted, resulting in an interrupt to the driver.

Note

The receive process remains in the running state.

Problem

When a Stop Receive command is issued during reception of a packet and a receive watchdog timeout error has occurred, CSR5<RWT> will not be set.

Implication

This anomaly is worked around in drivers for the DECchip 21041 developed by Digital.

In non-Digital developed drivers, CSR5<RWT> should not be used to check for the receive watchdog timeout condition and the suggested workaround should be implemented.

Workaround

The receive watchdog status reported in RDES0<RJ> should be used instead of CSR5<RWT>. Checking RDES0<RJ> is necessary only when CSR5<RWT> and CSR5<RI> have been set.

Capture-Effect Algorithm

Background

The capture-effect feature is enabled by setting CSR6 bit 17. In this mode, the DECchip 21041 selectively chooses between two types of backoff algorithms in order to prevent the capture-effect phenomena from occurring. The capture-effect is described in detail in Section 7.4.7 of the *DECchip 21041 PCI Ethernet LAN Controller Hardware Reference Manual*.

This feature to eliminate the capture-effect phenomena is not part of the IEEE 802.3 standard, but it works in conjunction with the standard protocol.

Problem

When working with an MAU that returns heartbeat signals, the 21041's capture-effect mode may not work as efficiently as indicated in the *DECchip 21041 PCI Ethernet LAN Controller Hardware Reference Manual*. The loss of efficiency occurs when only one transmission succeeds without collision following the backoff 2 or the backoff 0 stages.

The 21041's capture-effect mode will only work to its maximum efficiency following the backoff 2 or the backoff 0 stages if at least two packets are transmitted successfully.

Implication

Enabling the capture-effect mode on the DECchip 21041 does not eliminate the capture-effect phenomena. Instead it only reduces its effect.

Workaround

The heartbeat signal should be disabled whenever the capture-effect feature is used. In TP mode, disabling the heartbeat is done by disabling the signal quality pulse (CSR14<SQE> = 0). In non-TP modes, the MAU should be configured with the heartbeat signal disabled.

Auto-negotiation Support

Background

The IEEE 802.3 auto-negotiation algorithm can be used by Ethernet adapters to select between half- and full-duplex operation, and by Fast Ethernet adapters for 10/100 auto-negotiation.

Problem

The 21041's implementation of auto-negotiation does not support the latest draft (D4) of the IEEE standard.

Implication

The auto-negotiation feature should not be used.

Workaround

For information about future auto-negotiation support, please contact your Digital representative.

Underflow Reporting

Background

The following steps describe the 21041 transmit operation.

1. When the Tx process is running, data buffers are copied from host memory to the transmit FIFO, maintaining byte order. This means that unaligned buffers in the memory will also be unaligned in the FIFO. This can cause the following data structure in the transmit FIFO:

```
..........+-------+-------+-------+-------+
          |Byte 1 |xxxxxxx|xxxxxxx|xxxxxxx|  xxxxxxx - Represents
          +-------+-------+-------+-------+   unused data bytes
Buffer 1  |Byte 5 |Byte 4 |Byte 3 |Byte 2 |
          +-------+-------+-------+-------+
          |xxxxxxx|xxxxxxx|xxxxxxx|Byte 6 |
..........+-------+-------+-------+-------+
          |Byte 8 |Byte 7 |xxxxxxx|xxxxxxx|
          +-------+-------+-------+-------+
          |       |Byte 11|Byte 10|Byte 9 |
          +-------+-------+-------+-------+
Buffer 2  |       |       |       |       |
          +-------+-------+-------+-------+
          |       |       |       |       |
          +-------+-------+-------+-------+
          |xxxxxxx|Byte 23|Byte 22|Byte 21|
..........+-------+-------+-------+-------+
          |       |       |       |       |
          +-------+-------+-------+-------+
```

   The order for transmission of this data is from byte 1 to byte 23.

2. The "space counter" logic in 21041 counts FIFO entries, that is, longwords. This logic supplies the FIFO space information to other blocks. In the example in step 1, the "space counter" is aware of 8 entries that are occupied (there is no knowledge about the number of bytes with "real" information).

3. The 21041 starts transmitting a packet whenever the amount of data in the FIFO becomes larger than the programmed threshold (CSR6<TR>, which may be either 72, 96, 128 or 160 bytes).

   Whenever the "space counter" (multiplied by 4) becomes larger than the threshold, the 21041 starts transmitting. Potentially, as a result of non-longword-aligned information, transmission can begin prior to having enough "real" data bytes in the FIFO.

4. The "space counter" is incremented whenever a longword is added to the FIFO and decremented whenever the transmitter fetches an entry to be transmitted.

   Both the DMA and transmit logic sense the counter contiguously after 64 bytes (the collision window) have been transmitted (actual bytes).

   Prior to the collision window period, the transmit logic will fetch entries from the FIFO and transmit the data. It is aware of the non-real bytes and will transmit only the real ones. Because the minimal programmable threshold is larger than the collision window (72 bytes), no logic was required for processing an "underflow" which can never happen (if the entries are all full).

5. In the worst case, frames may be issued to 21041 in 1-byte buffers.

Problem

The underflow report problem occurs if the following two conditions are met:

1. If the space counter becomes larger than the programmed threshold, the transmit logic will start transmitting bytes (even if there are less than 64 real data bytes in the FIFO).
2. If all the bytes in the FIFO are transmitted and no additional bytes have been fetched from host memory, then the transmit logic will continue to fetch obsolete bytes from the FIFO and transmit them.

The underflow is not detected because the "space counter" is not sensed before the collision window is reached.

Implication

The anomaly with the underflow reporting is worked around in drivers for the DECchip 21041 developed by Digital.

In non-Digital developed drivers, one of the workarounds must be implemented to prevent the 21041 from transmitting a bad packet with a correct CRC onto the network without indicating the underflow error.

Workaround

There are several ways to work around the problem, depending on the format of the frame:

1. If the frame is distributed in longword-aligned buffers (whose length is also a multiple of 4), no "holes" will be created in the FIFO and no error will occur.
2. If #1 cannot be assumed, but the first buffer is guaranteed to be larger than 64 bytes (the collision window), not enough "holes" will be created in the FIFO and no error will occur.
3. If no assumptions can be made on the frame format, other than that the first buffer contains the data-link header (14 bytes), the driver must limit the number of buffers per frame according to the chosen threshold value, as listed in the following table:

Programmed Threshold	Maximum Buffers per Frame
72	1
96	9
128	17
160	31

Technical Support and Information

Digital is committed to assisting you with your integration of the DECchip 21041 Ethernet LAN Controller. For technical support and information, call the Digital Semiconductor Information Line:

United States and Canada	**1–800–332–2717**
TTY (United States only)	**1–800–332–2515**
Outside North America	**+1–508–568–6868**