Digital Semiconductor

EC–QC0CA–U1

DECchip 21140 PCI Fast Ethernet LAN Controller Hardware Reference Manual Update

This document provides updated information for the *DECchip 21140 PCI Fast Ethernet LAN Controller Hardware Reference Manual*, EC–QC0CA–TE.

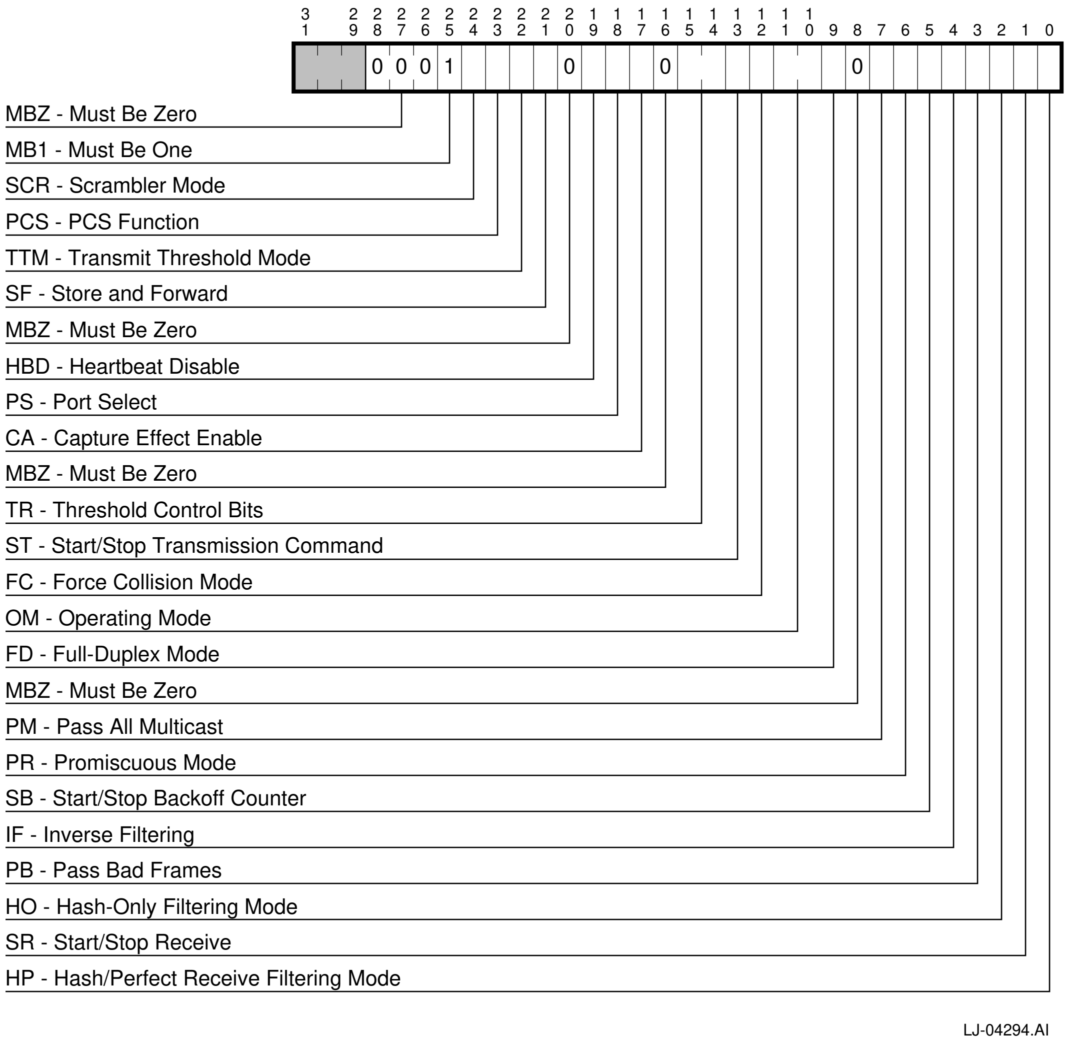
Section 3.2.2.5 Status Register (CSR5)

On page 3-26, in Table 3-35, **CSR5 Access Rules**, the value after reset should be changed as follows:

Category	Description
Value after reset	**FC000000H**

3.2.2.6 Operation Mode Register (CSR6)

On page 3-27, Figure 3-15, **CSR6 Operating Mode Register**, should show that bit 25 must be one. See the following figure for the correct information:


31 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 0 1 0 0 0
MBZ - Must Be Zero
MB1 - Must Be One
SCR - Scrambler Mode
PCS - PCS Function
TTM - Transmit Threshold Mode
SF - Store and Forward
MBZ - Must Be Zero
HBD - Heartbeat Disable
PS - Port Select
CA - Capture Effect Enable
MBZ - Must Be Zero
TR - Threshold Control Bits
ST - Start/Stop Transmission Command
FC - Force Collision Mode
OM - Operating Mode
FD - Full-Duplex Mode
MBZ - Must Be Zero
PM - Pass All Multicast
PR - Promiscuous Mode
SB - Start/Stop Backoff Counter
IF - Inverse Filtering
PB - Pass Bad Frames
HO - Hash-Only Filtering Mode
SR - Start/Stop Receive
HP - Hash/Perfect Receive Filtering Mode
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On page 3-28, in Table 3-36, **CSR6 Operating Mode Register Description**, update bits 28 through 25 as follows:

Field	Description
28:26	**MBZ — Must Be Zero**
	These bits are not used by the 21140 and should always be programmed to zero.
25	**MBO — Must Be One**
	This bit should always be programmed to one.

On page 3-31, in Table 3-36, **CSR6 Operating Mode Register Description**, add the following note to the description for bit 0:

Field	Description
0	**HP — Hash/Perfect Receive Filtering Mode (Read Only)**
	When reset, the 21140 does a perfect address filter of incoming frames according to the addresses specified in the setup frame (Table 4-8).
	When set, the 21140 does imperfect address filtering of multicast incoming frames according to the hash table specified in the setup frame. If CSR6<2> is set, then physical addresses are imperfect address filtered too. If CSR6<2> is reset, physical addresses are perfect address filtered, according to a single physical address, as specified in the setup frame.

Note

A unique condition occurs in hash/perfect receive filtering mode when a physical address is perfect filtered by comparing it to a single address. In this case, while in perfect filtering mode, the driver sends a setup frame containing the single physical address. The driver then sets the pass all multicast mode.

On page 3-32, following Table 3-37, **Transmit Threshold**, add the following note:

		Threshold (Bytes)	
CSR6<21>	**CSR6<15:14>**	**CSR6<22> = 0**	**CSR6<22> = 1**
0	00	128	72
0	01	256	96
0	10	512	128
0	11	1024	160
1	XX	Store and forward	Store and forward

Note

The CSR6<22> bit is meaningful only if the CSR6<18> bit is set. Otherwise, the threshold value remains as listed in the column with heading CSR6<22> = 1.

On page 3-33, in Table 3-39, **Loopback Operation Mode**, update footnote 1 as follows:

CSR6<11:10>	Operation Mode
01[1]	Internal loopback

[1]Internal loopback is performed on the serial and MII/SYM ports. If enabled by CSR6, it **also** tests the PCS functions (CSR6<23>) and the scrambler function (CSR6<24>). **Note that when internal loopback is performed on the SYM port, symbols appear on the network. When internal loopback is performed on the MII port, the mii_txen signal is disabled.**

Section 3.2.2.7 Interrupt Enable Register (CSR7)

On page 3-38, in Table 3-43, **CSR7 Access Rules**, the value after reset should be changed as follows:

Category	Description
Value after reset	**FFFE0000H**

Section 3.2.2.9 Serial Address ROM and MII Management Register (CSR9)

On page 3-42, in Table 3-47, **CSR9 Access Rules**, the value after reset should be changed as follows:

Category	Description
Value after reset	**FFF097FFH**

Section 4.2.2.2 Transmit Descriptor 1 (TDES1)

On page 4-16, in Table 4-7, **TDES1 Transmit Descriptor 1 Description**, add the following information to the description for bit 31:

Field	Description
31	**IC — Interrupt on Completion** When set, the 21140 sets transmit interrupt (CSR5<0>) after the present frame has been transmitted. It is valid only when last segment (TDES1<30>) is set **or when it is a setup packet**.

Section 5.2 Bus Commands

On page 5-2, in Table 5-1, **Bus Commands**, the last four commands should be changed as follows:

c_be_l<3:0>	Command	Type of Support
1100	**Memory read multiple**	**Supported as target**
1101	**Dual address cycle**	Not supported
1110	**Memory read line**	**Supported as target**
1111	**Memory write and invalidate**	**Supported as target**

Section 6.4 Loopback Operations

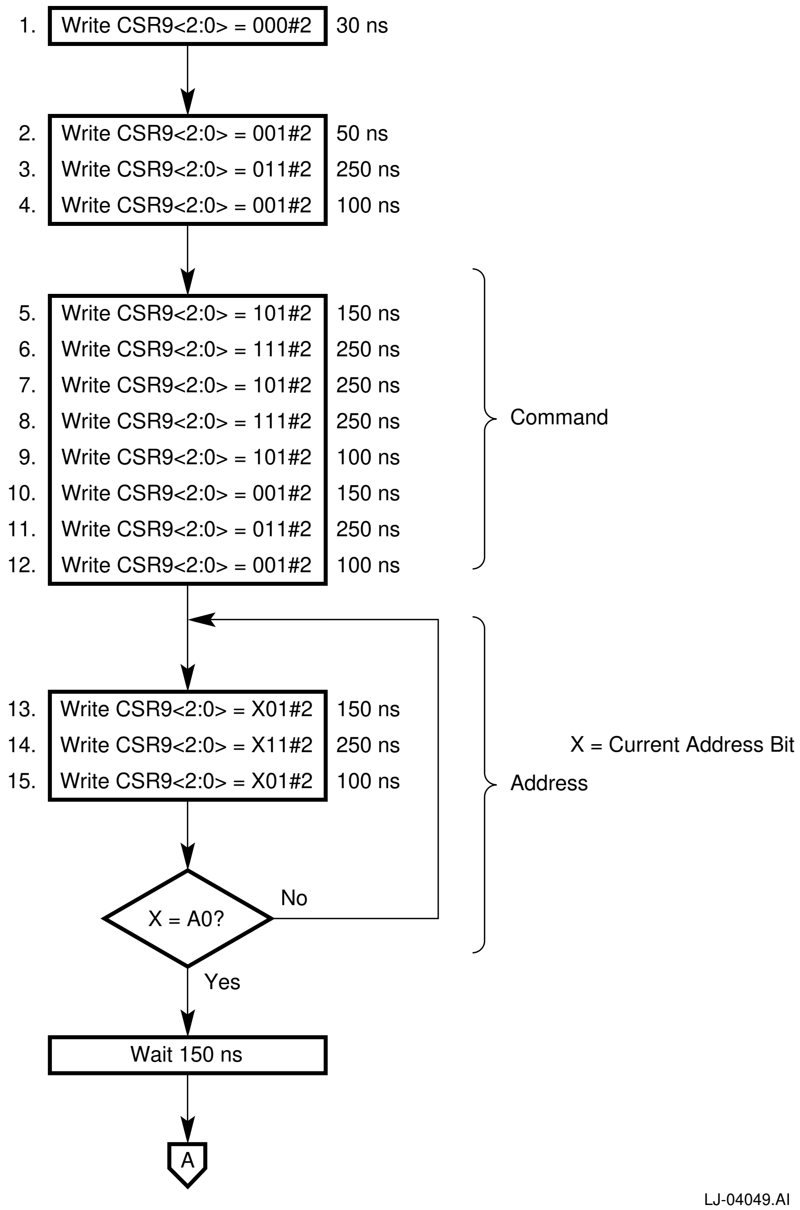
On page 6-19, in Section 6.4, **Loopback Operations**, change the last sentence, which reads ‘‘The loopback data rate is 10 Mb/s.’’, to the following: **The default value of the loopback data rate is 10 Mb/s. When the MII/SYM port is enabled, the loopback data rate is 100 Mb/s**.

Section 6.4.2 External Loopback Mode

On page 6-19, in Section 6.4.2, **External Loopback Mode**, delete the last sentence which reads as follows: ‘‘The 21140 should be in full-duplex mode (CSR6<9>).’’

Section 7.2.1 Read Operation

On page 7-3, in Section 7.2.1, **Read Operation**, replace the figure shown in Figure 7-2 Read Cycle (Page 1 of 2) with the following figure:


1. Write CSR9<2:0> = 000#2 30 ns
2. Write CSR9<2:0> = 001#2 50 ns
3. Write CSR9<2:0> = 011#2 250 ns
4. Write CSR9<2:0> = 001#2 100 ns
5. Write CSR9<2:0> = 101#2 150 ns
6. Write CSR9<2:0> = 111#2 250 ns
7. Write CSR9<2:0> = 101#2 250 ns
8. Write CSR9<2:0> = 111#2 250 ns
9. Write CSR9<2:0> = 101#2 100 ns
10. Write CSR9<2:0> = 001#2 150 ns
11. Write CSR9<2:0> = 011#2 250 ns
12. Write CSR9<2:0> = 001#2 100 ns
Command
13. Write CSR9<2:0> = X01#2 150 ns
14. Write CSR9<2:0> = X11#2 250 ns
15. Write CSR9<2:0> = X01#2 100 ns
X = Current Address Bit
Address
X = A0?
No
Yes
Wait 150 ns
A
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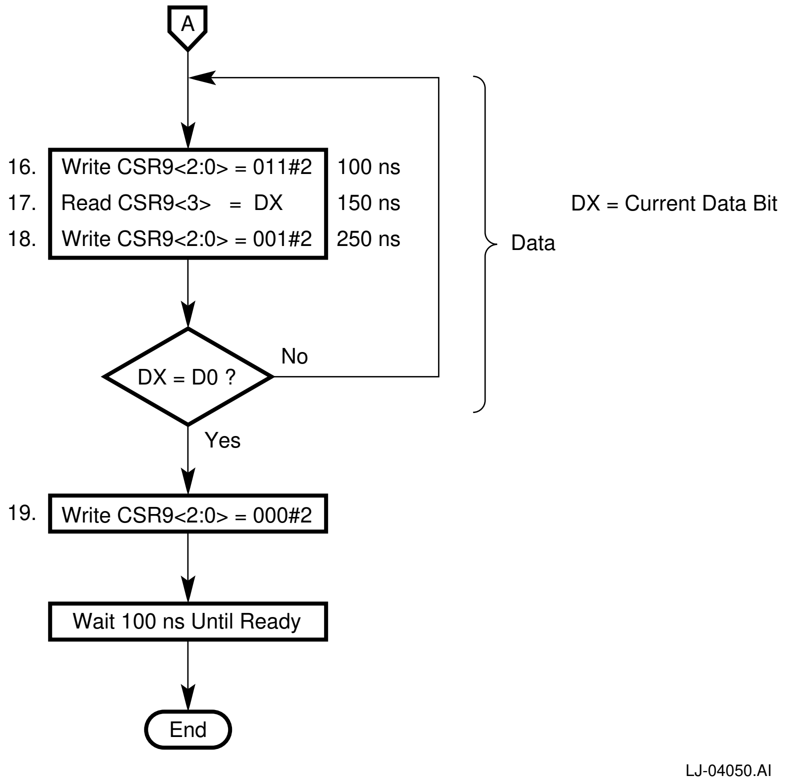
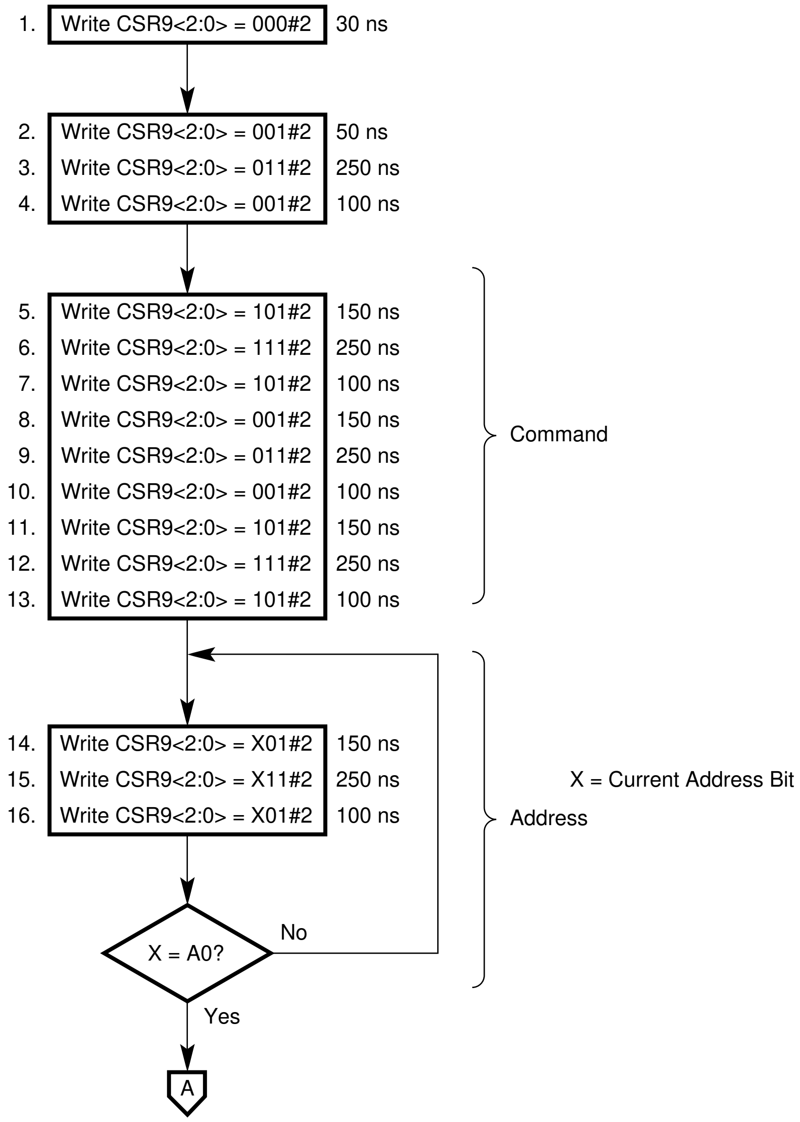
On page 7-4, in Section 7.2.1, **Read Operation**, replace the figure shown in Figure 7-3 Read Cycle (Page 2 of 2) with the following figure:



Section 7.2.2 Write Operation

On page 7-6, in Section 7.2.2, **Write Operation**, replace the figure shown in Figure 7-5 Write Cycle (Page 1 of 2) with the following figure:


1. Write CSR9<2:0> = 000#2 30 ns
2. Write CSR9<2:0> = 001#2 50 ns
3. Write CSR9<2:0> = 011#2 250 ns
4. Write CSR9<2:0> = 001#2 100 ns
5. Write CSR9<2:0> = 101#2 150 ns
6. Write CSR9<2:0> = 111#2 250 ns
7. Write CSR9<2:0> = 101#2 100 ns
8. Write CSR9<2:0> = 001#2 150 ns
9. Write CSR9<2:0> = 011#2 250 ns
10. Write CSR9<2:0> = 001#2 100 ns
11. Write CSR9<2:0> = 101#2 150 ns
12. Write CSR9<2:0> = 111#2 250 ns
13. Write CSR9<2:0> = 101#2 100 ns
Command
14. Write CSR9<2:0> = X01#2 150 ns
15. Write CSR9<2:0> = X11#2 250 ns
16. Write CSR9<2:0> = X01#2 100 ns
X = Current Address Bit
Address
X = A0?
No
Yes
A

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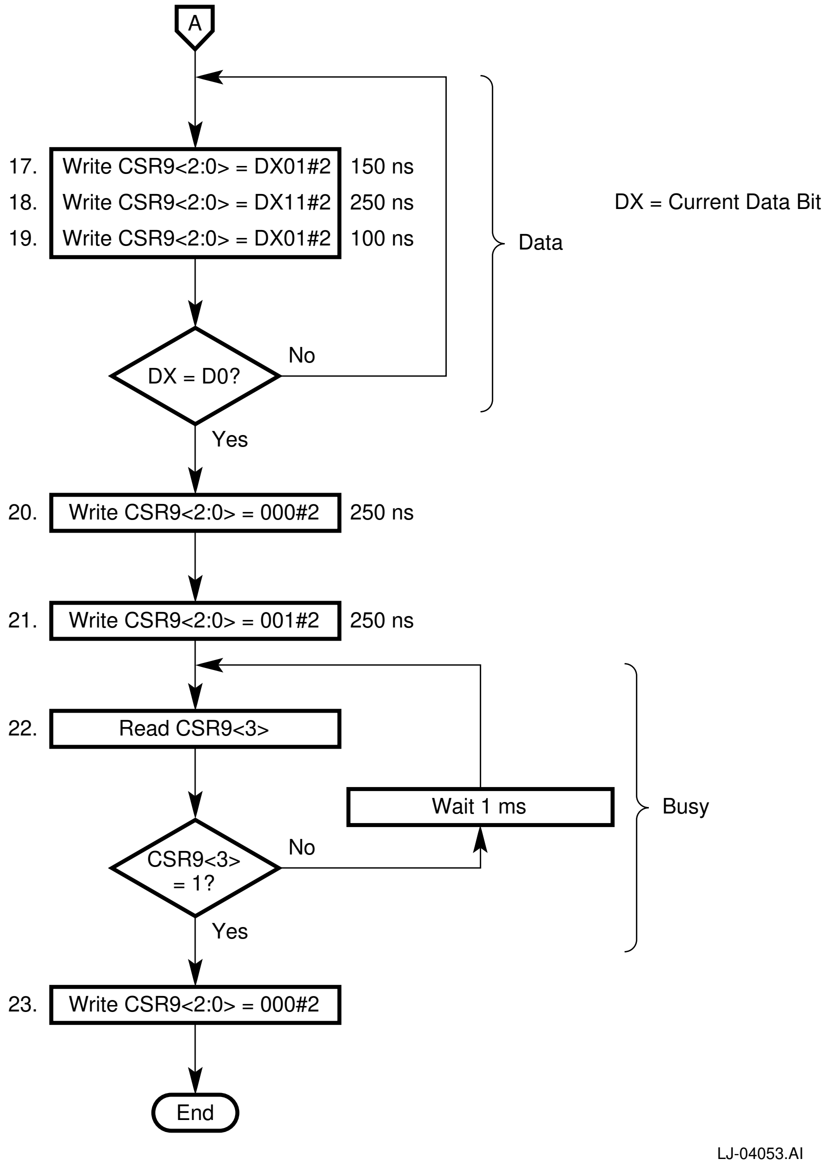
On page 7-7, in Section 7.2.2, **Write Operation**, replace the figure shown in Figure 7-6 Write Cycle (Page 2 of 2) with the following figure:



Appendix A.2.3 Boundary-Scan Register

On page A-3, in Appendix A.2.3, **Boundary-Scan Register**, change the boundary-scan register listing to read as follows (change clk to pci_clk, do$pd to sr_do, di$br to sr_di, sk_br to sr_ck, and cs_$br to sr_cs):

```
-> tdi          -> int_l       -> rst_l       -> pci_clk     -> gnt_l
-> req_l        -> ad_oe       -> ad<31:24>   -> cbe_oe      -> c_be_l<3>
-> idsel        -> ad<23:16>   -> c_be_l<2>   -> frame_oe    -> frame_l
-> irdy_oe      -> irdy_l      -> trdy_oe     -> trdy_l      -> devsel_oe
-> devsel_l     -> stop_oe     -> stop_l      -> perr_oe     -> perr_l
-> serr_l       -> par_oe      -> par         -> c_be_l<1>   -> ad<15:8>
-> c_be_l<0>    -> ad<7:0>     -> sr_do       -> sr_di       -> sr_ck
-> sr_cs        -> tdo
```